



STIC Search Report

EIC 2100

STIC Database Tracking Number: 105590

**TO: Alex Yufa
Location: PK2 4D21
Art Unit : 2133
Thursday, October 16, 2003**

Case Serial Number: 09888708

**From: Carol Wong
Location: EIC 2100
PK2-4B33
Phone: 305-9729**

carol.wong@uspto.gov

Search Notes

Dear Examiner Yufa,

Attached are the search results (from commercial databases) for your case.

Color tags mark the patents/articles which appear to be most relevant to the case.

Please call if you have any questions or suggestions for additional terminology, or a different approach to searching the case.

Thanks,
Carol



STIC Search Results Feedback Form

cw

EIC 2100

Questions about the scope or the results of the search? Contact *the EIC searcher or contact:*

Anne Hendrickson, EIC 2100 Team Leader
308-7831, CPK2-4B40

Voluntary Results Feedback Form

➤ I am an examiner in Workgroup: Example: 2100

➤ Relevant prior art **found**, search results used as follows:

- ☐ 102 rejection
- ☐ 103 rejection
- ☐ Cited as being of interest.
- ☐ Helped examiner better understand the invention.
- ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
(journal articles, conference proceedings, new product announcements etc.)

➤ Relevant prior art **not found**:

- ☐ Results verified the lack of relevant prior art (helped determine patentability).
- ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2100 CPK2-4B40



File 347:JAPIO Oct 1976-2003/Jun(Updated 031006)

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File 350:Derwent WPIX 1963-2003/UD,UM &UP=200366

(c) 2003 Thomson Derwent

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Set	Items	Description
S1	2767822	TIME OR TIMING OR TIMER? ? OR CLOCK??? ? OR TEMPORAL
S2	1786305	MINUTE? ? OR SECOND? ?
S3	358290	S1:S2(3N) (INTERVAL? ? OR PHASE OR PHASES OR ZONE OR ZONES - OR PERIOD? ? OR CYCLE OR CYCLES OR SECTOR? ? OR DURATION? OR - STAGE OR STAGES)
S4	345299	SAMPLE? OR SAMPLING?
S5	2257	ECC OR EDAC
S6	2961968	INVALID? OR MISTAK? OR FAIL? OR PROBLEM? OR FAULT? OR DEFE- CT? OR DEFICIEN? OR ABNORMA? OR FLAW? OR ABERRA? OR MALFUNCTI- ON?
S7	748243	INOPERA? OR UNUSUAL OR DYSFUNCTION? OR DISFUNCTION? OR BUG? ? OR DETERIORAT? OR ATYPICAL? OR ERROR? ? OR DEVIA? OR IRREG- ULAR? OR CORRUPT?
S8	243739	IMBALANC? OR EXCEPTION? ? OR DISTORT? OR DEGRAD? OR DISPAR- AT?
S9	218569	S6:S8(3N) (DETECT? OR DISCERN? OR FIND??? ? OR FOUND OR UNC- OVER? OR UN()COVER? OR CHECK? OR CHEQU? OR DIAGNOS? OR LOOK??? ? OR SEEK??? ?)
S10	49285	S6:S8(3N) (PROBE? ? OR PROBING OR SEARCH? OR ESTIMAT? OR EV- ALUAT? OR SURVEY? OR ANALYS? OR ANALYZ? OR ANALYT? OR ASSESS? OR EXAMIN? OR LOCAT? OR REVIEW? OR IDENTIFIC? OR IDENTIFIE? OR IDENTIFY?)
S11	23954	S6:S8(3N) (DISCRIMINAT? OR SCRUTIN? OR DIFFERENTIAT? OR SCR- EEN? OR PINPOINT? OR PIN()POINT??? ? OR RECOGNIT? OR RECOGNIS? OR RECOGNIZ?)
S12	67068	S6:S8(3N) (ASCERTAIN? OR INSPECT? OR DISTINGUISH? OR MONITO- R? OR TRACK? OR TROUBLESHOOT? OR TROUBLE()SHOOT? OR SCAN OR S- CANS OR SCANN??? ? OR TEST??? ?)
S13	451	SELFTEST? OR SELFDIAGNOS? OR BIST
S14	598595	IC OR ICS OR INTEGRAT?? ?(1W) (CIRCUIT? OR OPTOELECTRONIC? - OR OPTO()ELECTRONIC? ?) OR CHIP OR CHIPS OR MICROCIRCUIT? OR - MICROELECTRONIC? ?
S15	93962	MICRO() (CIRCUIT? OR ELECTRONIC? ?) OR PRINTED(1W)CIRCUIT? - OR MICROCHIP?
S16	66431	ASI OR ASIC OR VLSI OR VLSIC OR ULSI OR ULSIC OR VHSI OR V- HSIC OR SOI OR SOIC OR MSI OR MSIC OR LSI OR LSIC
S17	12483	S3 AND (S5 OR S9:S13)
S18	639	S17 AND S14:S16
S19	59	S18 AND S4
S20	56811	S4(3N) (DATA OR INPUT? OR SIGNAL? ? OR TRAFFIC? OR DATASTRE- AM? OR STREAM?)
S21	9880	BER OR BERT OR (BIT OR BITS OR MULTIBIT? ?) (2N)ERROR?
S22	19	S18 AND S20
S23	10	S18 AND S21
S24	8500	S3(10N)S4
S25	26	S18 AND S24
S26	30063	IC='H04L-001'
S27	188	MC='W01-A01C1':MC='W01-A01C1C'
S28	6857	MC='W01-A01'
S29	74	MC='W01-A01X'
S30	167	MC='T03-A02C5B'
S31	239	MC='W04-G01F1'
S32	14	MC='W02-G03J1C'
S33	250	MC='W02-G03J5'

S34 11151 IC='G11B-020/18'
 S35 9 MC='W02-G03J5C'
 S36 40 (S26 OR S34) AND S3 AND S14:S16
 S37 7 S36 AND S4
 S38 12 (S27:S33 OR S35) AND S3 AND S14:S16
 S39 42 S22:S23 OR S37:S38
 S40 42 IDPAT (sorted in duplicate/non-duplicate order)
 S41 42 IDPAT (primary/non-duplicate records only)
 ? t41/9/2-3,5,7,10

41/9/2 (Item 2 from file: 350)
 DIALOG(R)File 350:Derwent WPIX
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014387112 **Image available**
 WPI Acc No: 2002-207815/200227
 XRPX Acc No: N02-158454

Communication quality measurement method for code division multiple access cellular system, involves deriving desired signal power and interference signal power from eigen value of matrix
 Patent Assignee: NTT DOCOMO INC (NITE); NTT IDO TSUSHINMO KK (NITE);
 IMAI T (IMAI-I); MORI S (MORI-I)
 Inventor: IMAI T; MORI S
 Number of Countries: 031 Number of Patents: 007
 Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1143632	A2	20011010	EP 2001303248	A	20010405	200227 B
AU 200135063	A	20011011	AU 200135063	A	20010406	200227
CN 1322074	A	20011114	CN 2001122112	A	20010406	200227
JP 2001352275	A	20011221	JP 200153033	A	20010227	200227
KR 2001098471	A	20011108	KR 200118400	A	20010406	200227
US 20010030991	A1	20011018	US 2001827800	A	20010406	200227
AU 754356	B	20021114	AU 200135063	A	20010406	200303

Priority Applications (No Type Date): JP 200153033 A 20010227; JP 2000105485 A 20000406; JP 2000105486 A 20000406

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 1143632	A2	E 67	H04B-001/707	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
AU 200135063	A		H04Q-007/22	
CN 1322074	A		H04J-013/02	
JP 2001352275	A	37	H04B-001/707	
KR 2001098471	A		H04B-001/69	
US 20010030991	A1		H04K-001/00	
AU 754356	B		H04Q-007/22	Previous Publ. patent AU 200135063

Abstract (Basic): EP 1143632 A2

NOVELTY - A pair of data series consisting of time series data of a detected value and a delayed data with respect to reception **chip** time of a channel being measured, are generated. A covariant matrix of data series is derived. A desired signal power and interference signal power in the reception **chip** timing are derived from eigen value of matrix, to obtain SIR at reception **chip** timing.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

- (a) Communication quality measurement apparatus;
- (b) Synchronization detection method;
- (c) Synchronization detection device

USE - For measuring the quality in a mobile communication system

using code division multiple access cellular system.

ADVANTAGE - Measures the quality of communication with high precision and accuracy by considering all **chip** timing in a range set at a reception **chip** timing. Reliably detects synchronization with high speed, precision even when transmit diversity is applied. Measures SIR precisely using simple method without restricting **sample** number and **sampling interval** in series in **time** division for multiple channels.

DESCRIPTION OF DRAWING(S) - The figure shows an overall construction of wide band code division multiple access mobile communication system.

pp; 67 DwgNo 2/42

Title Terms: COMMUNICATE; QUALITY; MEASURE; METHOD; CODE; DIVIDE; MULTIPLE; ACCESS; CELLULAR; SYSTEM; DERIVATIVE; SIGNAL; POWER; INTERFERENCE; SIGNAL ; POWER; EIGEN; VALUE; MATRIX

Derwent Class: W01; W02

International Patent Class (Main): H04B-001/69; H04B-001/707; H04J-013/02; H04K-001/00; H04Q-007/22

International Patent Class (Additional): H04B-007/216; H04B-007/26; H04B-017/00; **H04L-001/20** ; H04L-007/00; H04Q-007/34

File Segment: EPI

Manual Codes (EPI/S-X): W01-B05A1A; W02-C03C1A; W02-C05; W02-K05A7; W02-K05B1

41/9/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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014212396 **Image available**

WPI Acc No: 2002-033093/200204

XRPX Acc No: N02-025426

Phase error detection circuit for application preset IC , has shift register responsive to output of divider alignment selector to generate phase error signal, when frequency divider is not switching in correct cycle

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: BRONSON T C; RUDOLPH B G

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6182237	B1	20010130	US 98144758	A	19980831	200204 B

Priority Applications (No Type Date): US 98144758 A 19980831

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6182237	B1		15	G06F-001/12	

Abstract (Basic): US 6182237 B1

NOVELTY - A divider alignment selector (130) multiplexes the output of frequency divider (120) and shift register (124) clocked in slow time domain. Shift register (124) clocked in the fast time domain is responsive to the output of selector (130) to generate a phase error signal when the phase alignment is incorrect or when frequency divider is not switching in a correct cycle.

DETAILED DESCRIPTION - The phase **error detection** circuit has a shift register (122) responsive to the output of a frequency divider (120) and clocked in the slow time domain for sequentially sampling for all possible alignments of the clock signals operating in slow time domain. A divider alignment selector (130) multiplexes the output of

the frequency divider and the shift register (122). A state machine logic (126,128,119) sequentially selects frequency divider output and **samples** the phase error **signal** for reporting a phase error, when each possible alignment results in activation of the phase error signal. INDEPENDENT CLAIMS are also included for the following:

- (a) **Clock** signal **phase** misalignment detecting method;
- (b) Recording medium

USE - Used in application specific **integrated circuit chips** (**ASIC**) e.g. microprocessors, memory controller **chips** , input-output bridge **chips** .

ADVANTAGE - Provides an improves circuit and method to **detect clock phase** alignment **errors** . Provides correct **failure** isolation. **Detects** phase alignment **errors** in an **ASIC** such as those arising from circuit failure or incorrect PLL initialization. Does not require special requirements for logic synthesis and timing tools. Does not require custom design techniques and embedded analog circuits.

DESCRIPTION OF DRAWING(S) - The figure shows logic diagram illustrating the phase **error** **detection** circuit.

Frequency divider (120)
Shift registers (122,124)
State machine logic (126,128,119)
Divider alignment selector (130)
pp; 15 DwgNo 2A/5

Title Terms: PHASE; ERROR; DETECT; CIRCUIT; APPLY; PRESET; **IC** ; SHIFT; REGISTER; RESPOND; OUTPUT; DIVIDE; ALIGN; SELECT; GENERATE; PHASE; ERROR; SIGNAL; FREQUENCY; DIVIDE; SWITCH; CORRECT; CYCLE

Derwent Class: T01; U22

International Patent Class (Main): G06F-001/12

File Segment: EPI

Manual Codes (EPI/S-X): T01-F02C1; T01-G02A1; T01-H01D; T01-K; T01-M05; T01-S03; U22-D03C; U22-D05A

41/9/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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013955883 **Image available**

WPI Acc No: 2001-440097/200147

Related WPI Acc No: 2001-520834

XRFX Acc No: N01-325441

Programmable timing **circuit** for testing cycle time of functional circuits on **IC** chip , has comparator to output signal indicating delay path longer than control path, after comparison of control and sample latches

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: BISHOP J W; FAX G A; ISEMINGER R G

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6219813	B1	20010417	US 98106959	A	19980629	200147 B

Priority Applications (No Type Date): US 98106959 A 19980629

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6219813	B1	14	G06F-011/00	

Abstract (Basic): US 6219813 B1

NOVELTY - A selectable input **signal** source is passively **sampled**

. A minimally delayed control path (112) includes a control latch (116). A programmable sub-cycle delay path (110) parallel to the control path, includes a sample latch (114). The state of the control and sample latches is compared by a comparator (118), and signal indicating the delay path longer than the control path, is output.

USE - For testing **cycle time** of functional circuits on **integrated circuit chip**.

ADVANTAGE - Provides on-**chip** test circuit for facilitating hardware based **cycle time** (HBCT) activities. Provides improved method for HBCT analysis in the determination of sort points. Provides improved capabilities for testing functional circuits following dicing and mounting of the **chips** to substrates. Provides functional circuit testing capability not requiring test equipment external to the **chip**.

Detects the **failure** of an object path, as its **clock cycle** is gradually shortened.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of on-**chip** programmable timing circuit.

Programmable sub-cycle delay path (110)

Minimally delayed control path (112)

Sample latch (114)

Control latch (116)

Comparator (118)

pp; 14 DwgNo 1/4

Title Terms: PROGRAM; TIME; CIRCUIT; TEST; CYCLE; TIME; FUNCTION; CIRCUIT;
IC ; **CHIP** ; COMPARATOR; OUTPUT; SIGNAL; INDICATE; DELAY; PATH; LONG;
CONTROL; PATH; AFTER; COMPARE; CONTROL; SAMPLE; LATCH

Derwent Class: T01; U21

International Patent Class (Main): G06F-011/00

File Segment: EPI

Manual Codes (EPI/S-X): T01-E04; T01-G02A1; T01-K01; U21-C01E

41/9/7 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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013486341 **Image available**

WPI Acc No: 2000-658284/200064

XRFX Acc No: N00-488078

Digital phase locked loop circuit used in magneto optical disc drive, synchronizes phase of regeneration clock and that of internal clock component in regenerated digital signal based on two phase error information

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000200467	A	20000718	JP 991690	A	19990107	200064 B

Priority Applications (No Type Date): JP 991690 A 19990107

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

JP 2000200467 A 10 G11B-020/14

Abstract (Basic): JP 2000200467 A

NOVELTY - The phase **error detector** (7) **detects** the phase **error** in signal output by reproducing single frequency area in the recording medium. A **tracking phase error detector** (8) **detects** phase **error** of digital **multibit** data signal. Based on the two phase error information, the **phase** of the regeneration **clock** and that of

the internal clock component in the regenerated digital signal are synchronized.

DETAILED DESCRIPTION - The band pair filter (4) removes direct flow component from the digital **data signal** obtained by **sampling** the **data** from single frequency area using an analog to digital convertor (11). The zero crossings of the output from band pair filter are detected by zero cross detector (5) whose output is zero flag which is counted as open starting point by a period counter (6). Based on the zero cross flag the phase **error detector** (7). **Detects** a phase **error** of digital output signal. A switching device (9) switches over either of the phase **error** signals from **detector** (7,8). The output of this switching device is filtered by a loop filter (10) whose output is converted by digital-analog convertor (11) based on which regeneration clock signal is provided by an oscillator (12).

USE - Digital phase locked loop circuit is used for clock regeneration in magneto-optical disc, optical disk drives e.g. for DVD-RAM.

ADVANTAGE - If the direct flow component exists in the reproduced signal, an exact phase **error** can be **detected**. As the frequency difference between regeneration clock and that of the clock component in the reproduced signal is large, high speed and speed and stable synchronization can be obtained. Less locking time can be achieved. Degradation of regeneration data quality by burst error etc., can be suppressed greatly by determining zero cross point of signal. Integration at the time of materializing an **IC** becomes simple and so the cost is reduced. Since PLL circuit is digitized. Clock regeneration suitable for PRML signal processing is possible.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of component of first embodiment of the digital phase locked looped circuit.

Band pair type filter (4)
Zero cross detector (5)
Period counter (6)
Phase **error detector** for harshness (7)
Switching device (9)
Loop filter (10)
Digital-analog convertor (11)
Oscillator (12)
pp; 10 DwgNo 1/9

Title Terms: DIGITAL; PHASE; LOCK; LOOP; CIRCUIT; MAGNETO; OPTICAL; DISC; DRIVE; PHASE; REGENERATE; CLOCK; INTERNAL; CLOCK; COMPONENT; REGENERATE; DIGITAL; SIGNAL; BASED; TWO; PHASE; ERROR; INFORMATION

Derwent Class: U22; U23; W01

International Patent Class (Main): G11B-020/14

International Patent Class (Additional): H03L-007/08; H04L-007/033

File Segment: EPI

Manual Codes (EPI/S-X): U22-H; U23-D01A3; U23-D01A8B; W01-A04A

41/9/10 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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012468040 **Image available**

WPI Acc No: 1999-274148/199923

XRFX Acc No: N99-205706

Phase error eliminating mechanism in data synchronizer - has control unit which restarts operation of VCO by applying calculated voltage for predetermined time due to which phase error detected by phase error detector is eliminated

Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11088170	A	19990330	JP 97250792	A	19970916	199923 B

Priority Applications (No Type Date): JP 97250792 A 19970916

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11088170	A		9	H03M-001/12	

Abstract (Basic): JP 11088170 A

NOVELTY - A control unit (19) restarts the operation of a voltage controlled oscillator (16). Voltage is applied immediately after restart of the oscillator by a **second** controller. The **period** of application by a first controller is immediately after passage of the set **time period**. DETAILED DESCRIPTION - **Phase** error of digital **signal** generated due to **sampling** is detected by a phase detector (12). A detector computes voltage to be applied to the oscillator and **time period** of application for eliminating the computed phase error. An INDEPENDENT CLAIM is included for the data synchronizing method.

USE - In data synchronizer, in **IC**.

ADVANTAGE - Locking of phase is performed at high speed.

DESCRIPTION OF DRAWING(S) - The figure shows the structure of data synchronizer. (16) Voltage controlled oscillator; (19) Control unit.

Dwg.1/4

Title Terms: PHASE; ERROR; ELIMINATE; MECHANISM; DATA; CONTROL; UNIT;
RESTART; OPERATE; VCO; APPLY; CALCULATE; VOLTAGE; PREDETERMINED; TIME;
PHASE; ERROR; DETECT; PHASE; ERROR; DETECT; ELIMINATE

Derwent Class: T01; U21; U23; W01

International Patent Class (Main): H03M-001/12

International Patent Class (Additional): G06F-003/05; H03L-007/08;
H04L-007/033

File Segment: EPI

Manual Codes (EPI/S-X): T01-C08; U21-A03; U23-D01A; W01-A04B1

? t41/9/11,13-14,16,18,20

41/9/11 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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012347086 **Image available**

WPI Acc No: 1999-153193/199913

Related WPI Acc No: 1998-239635

XRPX Acc No: N99-110466

Sampling clock generator for computer processor with large scale integrated system

Patent Assignee: HITACHI LTD (HITA)

Inventor: DOI T; HAYASHI T; NAKANO T

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5870594	A	19990209	US 94308346	A	19940919	199913 B
			US 97963857	A	19971104	

Priority Applications (No Type Date): JP 93232827 A 19930920

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5870594	A		17	G06F-001/06	Div ex application US 94308346 Div ex patent US 5737589

Abstract (Basic): US 5870594 A

NOVELTY - The sampling clock generator generates a **sampling** clock for latching **data** transmitted from an external device. The sampling clock timing is set up based on deviation between **sampling** clock and **data** transfer from the external device **detected** by a timing **error** **detector**

DETAILED DESCRIPTION - The latching of an input digital **signal** corresponding to the **sampling** clock timing is done by an input latch. A master clock signal is generated by a master clock generator (108) and based on which an address generator generates address of a memory **LSI chip**. The address generator has a selector (111). The inputs of the selector is from a tuning signal generator and a data transmitter (110) and a controller controls the selector to output the tuning signal during start up operation and the digital data during normal operation by applying sampling clock with different **periods**. The **timing error** detector has an **error discriminator** which compares the output of two exclusive-OR circuits and outputs an error signal.

USE - For high speed data transfer in **LSI** computer processor system.

ADVANTAGE - Deviation of timing between **data** transmitted and **sampling** clock is detected from the very latch used for **data sampling** and thereby high precision correction of clock timing is offered. Eliminates need for adjustment of correction during production and thereby higher speed production is performed owing to margin reduction.

DESCRIPTION OF DRAWING(S) - The figure is a block diagram of a data transfer system.

Master clock generator (108)

Data transmitter (110)

Selector (111)

pp; 17 DwgNo 1/4

Title Terms: SAMPLE; CLOCK; GENERATOR; COMPUTER; PROCESSOR; SCALE;

INTEGRATE; SYSTEM

Derwent Class: T01

International Patent Class (Main): G06F-001/06

File Segment: EPI

Manual Codes (EPI/S-X): T01-H07C; T01-K

41/9/13 (Item 13 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011141352 **Image available**

WPI Acc No: 1997-119276/199711

XRPX Acc No: N97-098195

Transceiver timing recovery in high-speed data transmission system - provides stable, min. bit error -rate, timing recovery algorithm for accurate sampling of incoming digital signals at symbol baud rate

Patent Assignee: TELEFONAKTIEBOLAGET ERICSSON L M (TELF)

Inventor: FERTNER A; SOELVE C; SOLVE T C J

Number of Countries: 071 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9703507	A1	19970130	WO 96SE942	A	19960711	199711 B
AU 9663761	A	19970210	AU 9663761	A	19960711	199724
			WO 96SE942	A	19960711	
US 5675612	A	19971007	US 95502317	A	19950713	199746
EP 839415	A1	19980506	EP 96923177	A	19960711	199822
			WO 96SE942	A	19960711	

CN 1195440	A	19981007	CN 96196715	A	19960711	199908
AU 709892	B	19990909	AU 9663761	A	19960711	199949
JP 2001505004	W	20010410	WO 96SE942	A	19960711	200128
			JP 97505758	A	19960711	

Priority Applications (No Type Date): US 95502317 A 19950713

Cited Patents: 4.Jnl.Ref; EP 330282; US 34206; US 4995031

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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WO 9703507	A1	E	52	H04L-007/02	
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Designated States (National): AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN

Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG

AU 9663761	A			H04L-007/02	Based on patent WO 9703507
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US 5675612	A		20	H04L-027/14	
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EP 839415	A1	E		H04L-007/02	Based on patent WO 9703507
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Designated States (Regional): DE FR GB IT SE

CN 1195440	A			H04L-007/02	
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AU 709892	B			H04L-007/02	Previous Publ. patent AU 9663761
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Based on patent WO 9703507

JP 2001505004	W		64	H04L-007/02	Based on patent WO 9703507
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Abstract (Basic): WO 9703507 A

Appts. for recovering **timing phase** and frequency of **sampling clock signal** in a receiver operates by minimising a mean square error due to a cancelled precursor inter-symbol interference. A **detected symbol error** is correlated with a signal obtd. from the input received signal. The correlation function approximates the timing instant where the mean squared error approaches its min., at which point an unambiguous zero-crossing of the correlation function signal may be obtd. From such unambiguity, i.e. only one clearly defined crossing, a required sampling timing instant may be determined.

USE/ADVANTAGE - Economic, **VLSI** -circuit appts. for efficiently tracking/adjusting phase-drift between transmitter and receiver clocks in e.g. ISDN network, correlating signals that avoid locking on to false zero-crossings, and avoiding oscillatory behaviour/susceptibility to spurious phenomena.

Dwg.2/13

Abstract (Equivalent): US 5675612 A

A timing recovery method in a digital communications system for determining a desired sampling instant in a digital receiver, comprising:

- sampling** a received **signal** at a controlled **sampling** instant;
- filtering the **sampled signal** in a filter;
- equalizing the filtered signal;
- detecting a symbol value corresponding to the **sampled signal** using the equalized signal;
- determining an error between the equalized signal and the detected symbol;

- controlling subsequent sampling instants by correlating the error with an unequalized signal obtained from the filter; and
- adjusting the sampling instant to minimize a magnitude of a correlation result.

Dwg.7/13

Title Terms: TRANSCEIVER; TIME; RECOVER; HIGH; SPEED; DATA; TRANSMISSION; SYSTEM; STABILISED; MINIMUM; BIT; ERROR; RATE; TIME; RECOVER; ALGORITHM; ACCURACY; SAMPLE; INCOMING; DIGITAL; SIGNAL; SYMBOL; BAUD; RATE

Derwent Class: W01

International Patent Class (Main): H04L-007/02; H04L-027/14

International Patent Class (Additional): H04L-025/38; H04L-027/16
File Segment: EPI
Manual Codes (EPI/S-X): W01-A01 ; W01-A04B2

41/9/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010665355 **Image available**
WPI Acc No: 1996-162309/199617
XRPX Acc No: N96-135977

Direct sequence spread spectrum digital radio link between fixed and mobile radio units - uses Tau dither phase control circuit or pilot jitter clock control circuit to control Rake fingers and clock phase adjuster of receiver

Patent Assignee: ROKE MANOR RES LTD (ROKE-N)
Inventor: HULBERT A P; KRUMPE A M
Number of Countries: 008 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2293730	A	19960403	GB 9419496	A	19940928	199617 B
EP 704985	A2	19960403	EP 95112921	A	19950817	199618
JP 8116292	A	19960507	JP 95251367	A	19950928	199628
FI 9504586	A	19960329	FI 954586	A	19950927	199635
US 5675616	A	19971007	US 95535355	A	19950928	199746
GB 2293730	B	19980805	GB 9419496	A	19940928	199833
EP 704985	B1	20020619	EP 95112921	A	19950817	200240
DE 69527123	E	20020725	DE 627123	A	19950817	200256
			EP 95112921	A	19950817	

Priority Applications (No Type Date): GB 9419496 A 19940928
Cited Patents: No-SR.Pub

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2293730	A		12	H04L-027/22	
EP 704985	A2 E		5	H04B-001/707	
Designated States (Regional): DE FR NL SE					
JP 8116292	A		4	H04B-001/707	
FI 9504586	A			H04B-007/01	
US 5675616	A		5	H04L-007/00	
GB 2293730	B			H04L-027/22	
EP 704985	B1 E			H04B-001/707	
Designated States (Regional): DE FR NL SE					
DE 69527123	E			H04B-001/707	Based on patent EP 704985

Abstract (Basic): GB 2293730 A

The appts for use in equipment providing a digital radio link between a fixed and a mobile radio unit has a Rake receiver with a number of Rake fingers. Each finger selectively receives the contents of each bit of a shift register. The shift register receives an analogue complex baseband signal via a **sample** and hold circuit and a digital to analogue converter. The **sample** and hold circuit receives a control signal from a **clock phase** adjuster circuit which is controlled by a controller according to an output signal received from each Rake finger.

Pref., each Rake finger includes a pilot correlator from which the output signal is generated. The controller is either a Tau dither phase control circuit or a pilot jitter phase control circuit.

USE/ADVANTAGE - Timing loop is closed around single Rake finger

which is experiencing strongest signal, which is **sampled** at only one **sample** per **chip** thereby rendering arbitrary timing of other Take fingers w.r.t. their multipath components.

Dwg.1/3

Abstract (Equivalent): US 5675616 A

A Rake receiver for use in equipment providing a digital radio link between a fixed and a mobile radio unit, comprising:

a **sample** and hold circuit for receiving an analog complex baseband signal;

an analog-to-digital converter connected to an output of the **sample** and hold circuit;

an output of the analog-to-digital converter connecting to a shift register;

outputs of the shift register connecting to a plurality of Rake fingers, each Rake finger having means for selectively receiving contents of each bit of said shift register; and

a control means for receiving outputs from said Rake fingers and for providing an output to a **clock phase** adjuster circuit for creating a control signal connected to said **sample** and hold circuit.

Dwg.1/3

Title Terms: DIRECT; SEQUENCE; SPREAD; SPECTRUM; DIGITAL; RADIO; LINK; FIX; MOBILE; RADIO; UNIT; TAU; DITHER; PHASE; CONTROL; CIRCUIT; PILOT; JITTER; CLOCK; CONTROL; CIRCUIT; CONTROL; RAKE; FINGER; CLOCK; PHASE; ADJUST; RECEIVE

Derwent Class: W01; W02

International Patent Class (Main): H04B-001/707; H04B-007/01; H04L-007/00; H04L-027/22

International Patent Class (Additional): H04B-007/005; H04B-007/02; H04B-007/216; H04B-007/26; **H04L-001/00**

File Segment: EPI

Manual Codes (EPI/S-X): W01-C01D3A; W02-C03C1C; W02-K05A1; W02-K05B3; W02-K08

41/9/16 (Item 16 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009941103 **Image available**

WPI Acc No: 1994-208815/199425

Related WPI Acc No: 1993-404134; 1994-332470

XRPX Acc No: N94-164279

High speed Integrated Circuit test appts - generates receive and transmit clocks using two preselected output pins and adjusts phase relation between clocks

Patent Assignee: RAMBUS INC (RAMB-N)

Inventor: GASBARRO J A; HOROWITZ M A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5325053	A	19940628	US 92894525	A	19920605	199425 B
			US 93110094	A	19930820	

Priority Applications (No Type Date): US 92894525 A 19920605; US 93110094 A 19930820

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5325053	A	14	G01R-031/00		Div ex application US 92894525 Div ex patent US 5268639

Abstract (Basic): US 5325053 A

The apparatus comprises a tester device for generating a **Tmultiplied byCLK** signal, an **Rmultiplied byCLK** signal, and a receive **data signal**. An **input sampling** device is coupled to receive the receive data signal over a bus **data pin**, the **input sampling** device generating an **input data** signal comprising a number of bits, the **input sampling** device coupled to transfer the input data signal to the **integrated circuit** device. A receive clock device generates an **RCLK** signal, such that the **RCLK signal** causes the **input sampling** device to **sample** the bus **data pin**. A shift device generates a transmit data signal over the bus data pin.

A transmit clock device generates a **TCLK** signal, such that the **TCLK** signal causes the shift device to shift the output data signal over the bus data pin and error logic device compares the input data input data signal and the output data signal to **detect** timing induced **errors**. Pref, the **IC** is a RAM composed of memory core(14) and a bus interface. The memory core is a DRAM.

USE/ADVANTAGE - Testing timing parameters of high speed **integrated circuits**. Data is transferred on both rising and falling edges of clock signals.

Dwg.8/10

Title Terms: HIGH; SPEED; INTEGRATE; CIRCUIT; TEST; APPARATUS; GENERATE; RECEIVE; TRANSMIT; CLOCK; TWO; PRESELECTED; OUTPUT; PIN; ADJUST; PHASE; RELATED; CLOCK

Derwent Class: S01; T01; U11; U14

International Patent Class (Main): G01R-031/00

File Segment: EPI

Manual Codes (EPI/S-X): S01-G01A1; T01-G02A2C; U11-F01C3; U14-A03B4; U14-D

41/9/18 (Item 18 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009114759 **Image available**

WPI Acc No: 1992-242193/199229

XRFX Acc No: N92-184716

DRAM on- chip error correction and detection - conducts error correction on entire row of memory during one error correction cycle when using memories which provide access to row of memory

Patent Assignee: HEWLETT-PACKARD CO (HEWP)

Inventor: RAYNHAM M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5127014	A	19920630	US 90479781	A	19900213	199229 B

Priority Applications (No Type Date): US 90479781 A 19900213

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

US 5127014 A 13 G06F-011/10

Abstract (Basic): US 5127014 A

The apparatus usable for **detection** of **errors** in a memory system of a computer has a random access memory device in the memory system. The memory device stores one or more rows of bits.

The **error detector** receives a second number of data bits and third number of **error** correction **bits** from the memory device. The second and the third number of bits are from accessing an entire row from one of the rows of bits from the memory device and providing a

first signal when an **error** is **detected** in the second number of bits. The second number of bits is detected in one detection **cycle**. The **second** number of bits are greater than the first such that the number of data **bits** on which **error detection** is performed is greater than the width of the data bus.

ADVANTAGE - Data within row of memory can be accessed independently of EC circuitry.

Dwg.4/6

Title Terms: DRAM; **CHIP**; ERROR; CORRECT; DETECT; CONDUCTING; ERROR; CORRECT; ROW; MEMORY; ONE; ERROR; CORRECT; CYCLE; MEMORY; ACCESS; ROW; MEMORY

Derwent Class: T01; U14

International Patent Class (Main): G06F-011/10

International Patent Class (Additional): G11C-029/00

File Segment: EPI

Manual Codes (EPI/S-X): T01-G01A1; T01-H01B3; T01-H01C4; U14-D02

41/9/20 (Item 20 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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008898500 **Image available**

WPI Acc No: 1992-025769/199204

XPX Acc No: N92-019571

Fault detection system for serial data - reduces simultaneous switching noise using net signal current with zero value

Patent Assignee: DIGITAL EQUIP CORP (DIGI)

Inventor: DUNCAN S H; SMELSER D W; WADE P C

Number of Countries: 006 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 4121444	A	19920116	DE 4121444	A	19910628	199204 B
GB 2247138	A	19920219	GB 9112157	A	19910606	199208
FR 2664110	A	19920103				199212
CA 2044051	A	19911230				199213
JP 6119197	A	19940428	JP 91151306	A	19910624	199422
GB 2247138	B	19941012	GB 9112157	A	19910606	199438
US 5481555	A	19960102	US 90546245	A	19900629	199607
			US 94206914	A	19940307	

Priority Applications (No Type Date): US 90546245 A 19900629; US 94206914 A 19940307

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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JP 6119197	A	14	G06F-011/00		
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GB 2247138	B	2	H04L-025/49		
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US 5481555	A	17	G06F-011/00	Cont of application US 90546245	
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Abstract (Basic): DE 4121444 A

The **fault detection** system provides a net signal current with a zero value over each cycle for reducing the simultaneous switching noise at the outputs of an **integrated circuit chip**. A coder codes each bit group within a word having a given bit length via a binary coding bit combination, each combinations of coding bits having the same number of binary '1' and binary '0' values.

USE - Serial data transmitted over relatively long distances.

(16pp Dwg.No.4/7

Abstract (Equivalent): GB 2247138 B

A system providing a net signalling current of substantially zero

at each **cycle time** thereby reducing a noise level for simultaneous switching outputs of an **integrated circuit chip**, the system comprising: an encoder that encodes an R bit input word to an S bit output word, and which encodes each of P groupings of M number of binary bits of the R bit input word to an even number of N encode binary bits to form the S bit output word, with each combination of the M number of binary bits being encoded according to one combination of N encode binary bits, the combinations of N encode binary bits including an equal number of binary '1' values and binary '0' values, with $P > 0$, $M > 0$, $R > 0$, N an even number > 1 , and N an even number $> M$.

Dwg.1/1

Abstract (Equivalent): US 5481555 A

A system for providing a net signalling current of substantially zero at each **cycle time** for reducing a noise level for simultaneous switching outputs of an **integrated circuit chip** and generating a signal having at least one **error detection bit**, the system comprising an encoder that encodes an R bit input word to an S bit output word, the encoder encoding each of P groupings of M number of binary bits of the R bit input word to an even number of N encode binary bits to form the S bit output word, the M number of binary bits being selected such that one P grouping of M number of binary bits includes binary bits of the R bit input word and at least one **error detection bit** for each byte of the R bit input word, the combinations of N encode binary bits including an equal number of binary '1' values and binary '0' values, with $P \text{ greater than } 0$, $M \text{ greater than } 0$, $R \text{ greater than } 0$, N an even number, and N an even number greater than M.

Dwg.8/8

Title Terms: FAULT; DETECT; SYSTEM; SERIAL; DATA; REDUCE; SIMULTANEOUS; SWITCH; NOISE; NET; SIGNAL; CURRENT; ZERO; VALUE

Derwent Class: U21; W01

International Patent Class (Main): G06F-011/00; H04L-025/49

International Patent Class (Additional): H03K-017/16; H03K-019/003;

H03M-007/14; H03M-013/02; H04B-015/00; H04L-001/00; H04L-029/14

File Segment: EPI

Manual Codes (EPI/S-X): U21-A06; U21-C02D; W01-A06A2

41/9/24 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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008483142 **Image available**
WPI Acc No: 1990-370142/199050
XRPX Acc No: N90-282225

Scan delay fault testing method for integrated circuits - has
driver which toggles its output on clock edge and on subsequent edge
receiver samples input

Patent Assignee: TEXAS INSTR INC (TEXI)

Inventor: WHETSEL L D

Number of Countries: 007 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 402134	A	19901212	EP 90306187	A	19900607	199050 B
US 5056094	A	19911008	US 89364915	A	19890609	199143
EP 402134	B1	19970903	EP 90306187	A	19900607	199740
DE 69031362	E	19971009	DE 631362	A	19900607	199746
			EP 90306187	A	19900607	
JP 3340736	B2	20021105	JP 90148894	A	19900608	200275

Priority Applications (No Type Date): US 89364915 A 19890609

Cited Patents: 2.Jnl.Ref; A3...9136; DE 3700251; NoSR.Pub; US 4672307

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 402134 A

Designated States (Regional): DE FR GB IT NL

EP 402134 B1 E 33 G06F-011/22

Designated States (Regional): DE FR GB IT NL

DE 69031362 E G06F-011/22 Based on patent EP 402134

JP 3340736 B2 31 G01R-031/317 Previous Publ. patent JP 3103781

Abstract (Basic): EP 402134 A

The test cell (12) comprises two memories, a flip-flop (24) and a latch (26), for storing test data. A multiplexer (22) selectively connects one of the inputs to the flip-flop (24). The input of the latch (26) is connected to output of the flip-flop (24). The output of the latch (26) is connected to one input of a multiplexer (28), the second input to the multiplexer (28) being a data input (DIN) signal. A control bus (17) is provided for controlling the multiplexers (22,28), flip-flop (24) and latch (26).

The test cell allows input data to be observed and output data to

be controlled simultaneously. A driving device (264) toggles its output on a clock edge. On a subsequent clock edge, the receiving circuit (266) **samples** its **input**. The **sampled input** may be scanned out and compared to the toggled value to determine whether the signal propagated between the first and second clock edges.

ADVANTAGE - Allows propagation delays between devices to be determined. (31pp Dwg.No.2/21

Abstract (Equivalent): EP 402134 B

Apparatus for testing the propagation delay between a driving device (12a-12d, 18, 264) and a receiving device (12e-12h, 20, 266), comprising a clock (CLK) for producing a plurality of clock pulses having first and second edges (272, 278, 282, 287, 288, 294); said driving device (12a-12d, 18; 264) for outputting a signal (DOUT; OUT) corresponding to a known value responsive to a first clock edge (272); said receiving device (12e-12h, 20; 266) for **sampling** the **signal** (DIN; IN) at an input of the receiving device responsive to said second clock edge (278); and circuitry for comparing said **sampled input** to expected **data** to determine whether said signal propagated to the receiving device (12e-12h, 20; 266) within the **time period** between said first and second edges (274, 278); characterised in that said driving device has test cell circuitry (12; 22-28) selectively operating in either a first mode for performing boundary scan testing or a second mode for outputting said signal corresponding to a known value responsive to a first clock edge (272); in that said receiving device has test cell circuitry (12, 22-28) selectively operating in either a first mode for performing boundary scan testing or a second mode for **sampling** said **signal** at an input of the receiving device responsive to said second clock edge (278); and in that said comparing circuitry comprises circuitry for comparing said **sampled input** to said known value in said second mode to determine as aforesaid whether said signal propagated to the receiving device within the **time period** between said first and second edges.

Dwg.1/22

Abstract (Equivalent): US 5056094 A

The test cell (12) provides boundary scan testing in an **integrated circuit** (10).

The test cell (12) comprises two memories, a flip-flop (24) and a latch (26), for storing test data.

A first multiplexer (22) selectively connects one of a number of inputs to the flip-flop (24).

The input of the latch (26) is connected to output of the flip-flop (24).

The output of the latch (26) is connected to one input of a multiplexer (28), the second input to the multiplexer (28) being a data input (DIN) signal.

A control bus (17) is provided for controlling the multiplexers (22,28), flip-flop (24) and latch (26). The test cell allows input data to be observed and output data to be controlled simultaneously.

This architecture allows propagation delays between devices to be determined.

A driving device (264) toggles its input on a first clock edge.

On a subsequent clock edge, the receiving circuit (266) **samples** its **input**. The **sampled input** may be scanned out and compared to the toggled value to determine whether the signal propagated between the first and second clock edges. USE - For **testing** delay **faults** between **ICs**.

(28pp

Title Terms: SCAN; DELAY; FAULT; TEST; METHOD; INTEGRATE; CIRCUIT; DRIVE; TOGGLE; OUTPUT; CLOCK; EDGE; SUBSEQUENT; EDGE; RECEIVE; SAMPLE; INPUT
Derwent Class: S01; U11

International Patent Class (Main): G01R-031/317; G06F-011/22
International Patent Class (Additional): G01R-031/28; G01R-031/30;
G06F-011/26
File Segment: EPI
Manual Codes (EPI/S-X): S01-G01A; U11-F01D2

41/9/25 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007978593 **Image available**
WPI Acc No: 1989-243705/198934
XRPX Acc No: N89-185724

IC analog-digital converter with error correction - has conversion
stage with two supplementary quantisation intervals giving logic value if
analog value is near border between two successive

Patent Assignee: THOMSON HYBRIDES MI (CSFC)

Inventor: THAO N T

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
FR 2625388	A	19890630	FR 8718298	A	19871229	198934 B

Priority Applications (No Type Date): FR 8718298 A 19871229

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
FR 2625388	A	15		

Abstract (Basic): FR 2625388 A

The converter with parallel - series configuration consists of at least two conversion stages (12,13), each comprising comparators which define 2 power n quantisation intervals of length q, over a voltage range 0 to V. The **second stage** (13) has two supplementary intervals, one situated at the bottom of its voltage scale (-1) and the other at the top of the scale (2 power n).

If an analog value (x1), applied to the first stage input is near the border between two successive intervals (i,i+1), the **error** is **detected** by the **second stage**, which receives the analog signal (x2) from the first stage into one of the two supplementary intervals. For signal x2 having a value between 0 and V the supplementary comparators give a logic signal 0, while for x2 out of this range, the logic signal is 1. Each stage delivers a logic number, b1 from the first and b2 from the second, the latter having a supplementary **bit** indicating the **error**. An adder sums up the two numbers, giving an exact logic number.

ADVANTAGE - Eliminates errors due to voltage values near limit of comparator quantisation intervals. Manufactured on GaAs or silicon chips .

7/8

Title Terms: IC ; ANALOGUE-DIGITAL; CONVERTER; ERROR; CORRECT; CONVERT;
STAGE; TWO; SUPPLEMENTARY; QUANTUM; INTERVAL; LOGIC; VALUE; ANALOGUE;
VALUE; BORDER; TWO; SUCCESSION

Derwent Class: U21

International Patent Class (Additional): H03M-001/16

File Segment: EPI

Manual Codes (EPI/S-X): U21-A03F

41/9/27 (Item 27 from file: 350)

DIALOG(R)File 350:Derwent WPIX
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007480218 **Image available**
WPI Acc No: 1988-114152/198817
XRPX Acc No: N88-086743

Reproducing appts. for PCM signal with muting circuit - produces error flags on output which cause control unit to switch on muting unit and generate auxiliary signals

Patent Assignee: PHILIPS GLOEILAMPENFAB NV (PHIG); BOSCH GMBH ROBERT (BOSC)

Inventor: HORSTEN J B

Number of Countries: 009 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 264986	A	19880427	EP 87201817	A	19870922	198817 B
NL 8602418	A	19880418				198819
US 4864573	A	19890905	US 8793452	A	19870904	198945
CA 1282168	C	19910326				199117
EP 264986	B1	19930113	EP 87201817	A	19870922	199302
DE 3783559	G	19930225	DE 3783559	A	19870922	199309
			EP 87201817	A	19870922	

Priority Applications (No Type Date): NL 862418 A 19860925

Cited Patents: EP 101180; EP 180764; GB 2107496; JP 580565; JP 58164005; JP 59004345; JP 60085469; JP 60136960; 05Jnl.Ref; JP 58056547

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 264986	A	E	15		
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Designated States (Regional): AT BE DE FR GB IT NL

US 4864573	A		13		
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EP 264986	B1	E	18	G11B-020/18	
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Designated States (Regional): AT BE DE FR GB IT NL

DE 3783559	G			G11B-020/18	Based on patent EP 264986
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Abstract (Basic): EP 264986 A

The appts. comprises error correction devices for errors in one or more of the data words forming the pcm signal. When the correction devices are no longer capable of correcting errors they produce error flags on an output that are applied to a control unit. From the error flags the control unit devices a control signal. The control signal is applied to a muting unit to turn the unit on.

The muting unit transfers the signal applied to its input to its output in the absence of a control signal. The muting unit holds the signal on its output at a specific fixed value for a specific **time interval** when the control signal is present on its control input.

USE - E.g. for compact disk players.

Dwg.4/6

Abstract (Equivalent): EP 264986 B

An apparatus for reproducing a pulse-code-modulated signal from a transmission channel, for example a track of a record carrier, which pulse-code-modulated signal is contained in a sequence of consecutive data words, comprising - a receiving means (1) for receiving the pulse-code-modulated signal from the transmission channel and for supplying the received signal to an input of - error-correction means (3) for correcting errors in one or more of the data words, comprising a first output (4) for supplying the data words, which may have been corrected, and a second output for supplying an error flag (7) if the error-correction means are no longer capable of correcting the error in the data word, - a control unit (9) having an input (8), coupled to the second output of the error-correction means, and an output (10), which

control unit comprises a counter, and which is constructed to count the error flags applied to its input, to generate a control signal in response to the error flags counted and to apply this control signal to its output, - a muting unit (6) having a signal input (5) coupled to the first output of the error-correction means, a control input (11) coupled to the output of the control unit, and an output (12), which muting unit is constructed to transfer the signal applied to its input to its output in the absence of the control signal on its control input and is constructed to hold the signal on its output at a specific fixed value for a specific **time interval** when the control signal is present on its control input, characterised in that the control unit (9) comprises N counters (22, 36), where $N > 2$, is that the first counter (22) is constructed to count the number of error flags appearing within a first **time interval** T_1 and is constructed to supply a first auxiliary signal (S1) after detection of n_1 error flags within the **time interval** T_1 , in that the i -th counter (36) is constructed to count the number of error flags appearing within an i -th **time interval** T_i which occurs after the instant at which the $(i-1)$ -th counter supplies the $(i-1)$ -th auxiliary signal, and is constructed to supply an i -th auxiliary signal (S2) after detection of n_i error flags within the **time interval** T_i , i ranging from 2 to N inclusive and n_1 to n_N being integers greater than or equal to 1, in that, in the case that a **time interval** T_1 or T_i lapses without the first or i -th counter respectively counting n_1 or n_i error flags, the control unit is adapted so as to restart said counting of error flags in the first **time interval** T_1 by said first counter, and in that the control unit further comprises a control-signal generator (43) having an input for receiving the N-th auxiliary signal and an output coupled to the output (10) of the control unit, which control-signal (Cs) generator is constructed to supply the control signal to its output for a **time interval** T_m which occurs after the instant at which the N-th auxiliary signal is received.

(Dwg.4/6

Abstract (Equivalent): US 4864573 A

A receiver (1) obtains the P.C.M. signal from the transmission channel, and it is then passed to an error corrector (3) in the form of data words which are corrected if possible. If corrected they are output to a control unit (9), and if they are unable to be corrected, they are output to a muting unit (6). The control unit generates a control signal in response to error flags supplied by the error corrector, and this is output to the muting unit. The muting unit supplies its signal to the output (13) if no control signal is being sent to it, but holds its signal at a specific fixed value, for a specific **time interval**, if a control signal is present. The control unit comprises N counters, where N is greater than or equal to 2. The first counter counts the error flags in a **time interval** T_1 , hence the control signal is held for a specific time and value. USE/ADVANTAGE - Error correction in compact disc players. Easily integrated, less space needed on **Integrated Circuit**. (13pp)

Title Terms: REPRODUCE; APPARATUS; PCM; SIGNAL; MUTE; CIRCUIT; PRODUCE; ERROR; FLAG; OUTPUT; CAUSE; CONTROL; UNIT; SWITCH; MUTE; UNIT; GENERATE; AUXILIARY; SIGNAL

Derwent Class: T03; W01; W04

International Patent Class (Main): G11B-020/18

International Patent Class (Additional): G06F-011/10; H03M-013/00;

H04N-005/94; H04N-009/88

File Segment: EPI

Manual Codes (EPI/S-X): T03-P01A; W01-A01 ; W04-G01

41/9/28 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007445226 **Image available**
WPI Acc No: 1988-079160/198812
XRPX Acc No: N88-060078

**Signal receiver for communication over electricity mains network -
predicts correlation coeffts. for received signals, compares to actual
correlation values, and determines sequence of coded data signals**

Patent Assignee: THORN EMI PLC (THOE)
Inventor: BURR A G; YOUNG N A
Number of Countries: 008 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 260851	A	19880323	EP 87307866	A	19870907	198812 B
US 4833694	A	19890523	US 8794842	A	19870910	198924
CA 1274595	A	19900925				199044
EP 260851	B1	19940629	EP 87307866	A	19870907	199425
DE 3750152	G	19940804	DE 3750152	A	19870907	199430
			EP 87307866	A	19870907	

Priority Applications (No Type Date): GB 8621875 A 19860911
Cited Patents: 1.Jnl.Ref; A3...8933; EP 88564; No-SR.Pub; US 3341658; US
4550414; US 4653069

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 260851	A	E	8		
Designated States (Regional): DE FR GB IT NL SE					
US 4833694	A		8		
EP 260851	B1	E	12	H04L-023/02	
Designated States (Regional): DE FR GB IT NL SE					
DE 3750152	G			H04L-023/02	Based on patent EP 260851

Abstract (Basic): EP 260851 A

The line network communication system transmits a series of coded data signals on a baseband carrier signal and has a receiver for recovering the coded data signals. The receiver operates in a search mode to compare a series of received data signals with coded reference signals at different relative phases. The comparison continues until at least one comparison signal indicates a correlation exceeding a threshold value.

A locking mode maintains a selected phase difference while the correlation exists to permit recovery of the coded signals. Actual correlation values are stored and multiplied by corresp. predicted correlation coeffts. and the resultant products are summed. The two summed values are compared to determine the identity of the sequence.

USE/ADVANTAGE - In system, e.g. for telecontrol, where each transmitted 'one' bit is represented by PRBS of 1024 'chips' and each 'nought' bit by second such sequence. Can be used for communication over noisy lines, improved correlation results.

6/6

Abstract (Equivalent): EP 260851 B

A line network communication system including a transmitter means capable of transmitting a series of data signals represented by signal sequences of first and second kinds on a baseband carrier signal and receiver means capable of receiving a transmitted signal and recovering therefrom said data signals, the receiver means being arranged to operate in a search mode to compare received signals with first and second reference sequences at different relative phases until at least one comparison signal generated as a result of the comparisons

indicates a degree of correlation exceeding a threshold value, the reference sequences corresponding to the signal sequences of the first and second kinds respectively, a track mode to verify that said degree of correlation exists for a preset **time interval** and, in dependence on a successful verification in the tracking mode, a locking mode to maintain a selected phase between the received signals and the reference sequences while said degree of correlation exists, permitting recovery of the data signals, characterised in that the receiver includes means (1) to predict correlation coefficients for the received signal sequences of the first and second kinds with the corresponding reference signal sequences at different relative phases, means to store corresponding actual correlation coefficients between a received signal sequence and the first and second reference sequences, and means (6, 7) to effect an analysis process in which the actual correlation coefficients stored are multiplied by the corresponding predicted correlation coefficients for both reference sequences, the two sets of resultant products, each set being related to a respective reference sequence, are individually summed, and the two summed sets are compared to determine the identity of the received signal sequence.

(Dwg.6/6

Abstract (Equivalent): US 4833694 A

The signal receiver, for use in a system for communication and telecontrol over the electricity mains network, has a correlation stage in which values of correlation coefficients for a received signal are predicted in a processor taking due account of known distortions of the network. Then these coefficients are multiplied, shifted and averaged with recent results to minimise the effects of noise, the consequent values being multiplied by the actual correlation values of the received signal in the bins for comparison. ADVANTAGE - Improved signal-to-noise ratio.

(8pp)

Title Terms: SIGNAL; RECEIVE; COMMUNICATE; ELECTRIC; MAINS; NETWORK; PREDICT; CORRELATE; COEFFICIENT; RECEIVE; SIGNAL; COMPARE; ACTUAL; CORRELATE; VALUE; DETERMINE; SEQUENCE; CODE; DATA; SIGNAL

Index Terms/Additional Words: POWER; LINE; CARRY

Derwent Class: W01; W02; W05; X12

International Patent Class (Main): H04L-023/02

International Patent Class (Additional): H04B-001/66; H04B-015/00; H04L-007/04

File Segment: EPI

Manual Codes (EPI/S-X): W01-A01 ; W02-C01A; W05-D05; X12-H03

41/9/29 (Item 29 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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007268546

WPI Acc No: 1987-265553/198738

Signal recorder on disc-shaped recording medium - controls speed of driving motor by using phase comparator, integrator circuit and motor drive circuit

Patent Assignee: SONY CORP (SONY)

Inventor: SAKO Y; YAMAGAMI T; YAMAMURA S

Number of Countries: 006 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 238194	A	19870923	EP 87301223	A	19870212	198738 B
JP 62192076	A	19870822	JP 8633322	A	19860218	198739
AU 8768719	A	19860820				198740
US 4829497	A	19890509	US 878780	A	19870130	198922

CA 1284381	C	19910521			199125
EP 238194	B1	19920513	EP 87301223	A	19870212 199220
DE 3778945	G	19920617	DE 3778945	A	19870212 199226
			EP 87301223	A	19870212
KR 9408691	B1	19940924	KR 871249	A	19870216 199633

Priority Applications (No Type Date): JP 8633322 A 19860218

Cited Patents: 5.Jnl.Ref; A3...8843; EP 129224; EP 130091; EP 137346; EP 137855; EP 158067; EP 18157; GB 2080997; GB 2082426; GB 2085199; GB 2088088; JP 58125209; JP 59154612; JP 60070505; JP 60087405; JP 60089861; No-SR.Pub; US 4355338; US 4382268

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 238194	A	E			
US 4829497	A		13		
EP 238194	B1	E	18	G11B-020/10	
DE 3778945	G			G11B-020/10	Based on patent EP 238194
KR 9408691	B1			G11B-020/12	

Abstract (Basic): EP 238194 A

The recording apparatus comprises a device circuit (36) for recognising each transmission rate of the time-sequential data and outputs a corresponding signal. A rotational speed controller (23 for 25) controls the speed of the disc-shaped recording medium (11) in response to the signal output from the **recogniser**. An **error** correcting code is generated (34) for the time-sequential digit data to be recorded in the sectors so as to correct a possible error which may occur in the digital data. The code is added to the digital data.

A recording signal generator (35) converts the digital data, to which is added the error correcting code, into a signal for recording in one or more sectors of the disc-shaped recording medium.

USE/ADVANTAGE - Audio signal or video signal. Possible to record over long **time period** without signal deterioration.

(Dwg. No.1

/5

Abstract (Equivalent): EP 238194 B

Apparatus for recording an input signal on one or more sectors of a disc-shaped recording medium (11) having a plurality of sectors, the apparatus being selectively supplied with time-sequential data having one of a plurality of predetermined transmission rates, the apparatus comprising: means (36) for recognising each transmission rate of said time-sequential data and for outputting a corresponding signal (REF); rotational speed control means (23 to 25) for controlling the rotational speed of said disc-shaped recording medium (11) in response to said signal (REF) output from said data transmission rate recognising means (36); means (34) for generating an error correcting code (**ECC**) for said time-sequential data to be recorded in said sectors so as to correct a possible error which may occur in said time-sequential data and for adding said error correcting code (**ECC**) to said time-sequential data; and recording signal generating means (35) for converting said time-sequential data to which is added said error correcting code (**ECC**) into a signal for recording in one or more sectors of said disc-shaped recording medium (11), said recording signal generating means (35) including means for recording the recording the signal on said disc-shaped recording medium (11) whose rotation is controlled by said rotational speed control means (23 to 25) in accordance with the data transmission rate of the time sequential data supplied to said apparatus; characterised in that: said means (36) for recognising the data transmission rate of said time-sequential data is operable to extract clock information included in said time-sequential data and to recognise the data transmission

rate on the basis of the extracted clock information; and said recording signal generating means (35) further includes means for recording an identification signal (1D) indicative of the data transmission rate in a directory allocated in a predetermined area of said disc-shaped recording medium (11).

Abstract (Equivalent): US 4829497 A

When a time-sequential signal such as an audio or digital data signal is optically recorded on a disc-shaped recording medium, the transmission rate of the digital data is determined or the time-sequential audio **signal** is **sampled** at a predetermined frequency to obtain time-sequential digital data which is sequentially recorded on the disc-shaped recording medium.

The rotational speed of the disc-shaped recording medium is controlled in response to the transmission rate of the time-sequential digital data. (13pp)

Title Terms: SIGNAL; RECORD; DISC; SHAPE; RECORD; MEDIUM; CONTROL; SPEED; DRIVE; MOTOR; PHASE; COMPARATOR; INTEGRATE; CIRCUIT; MOTOR; DRIVE; CIRCUIT

Derwent Class: T03; W04

International Patent Class (Main): G11B-020/10; G11B-020/12

International Patent Class (Additional): G11B-007/00; G11B-007/013;

G11B-015/52; G11B-019/24; G11B-019/28; **G11B-020/18** ; H04B-014/04

File Segment: EPI

Manual Codes (EPI/S-X): T03-F02; T03-N01; T03-P01A; W04-E02A

? t41/9/31-36

41/9/31 (Item 31 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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004817958

WPI Acc No: 1986-321299/198649

XRPX Acc No: N86-239623

Dual edge clock address mark detector - has generation of sync. signal controlled by decoder identifying which of two registers contains data and which contains clock

Patent Assignee: SMC STANDARD MICROSYSTEMS CORP (SMCS-N)

Inventor: LI T P; PECHAR H W

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2175776	A	19861203	GB 866087	A	19860312	198649 B
US 4625321	A	19861125	US 85737060	A	19850523	198650
JP 61273014	A	19861203	JP 8641370	A	19860226	198703

Priority Applications (No Type Date): US 85737060 A 19850523

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
GB 2175776	A	5		

Abstract (Basic): GB 2175776 A

An input receives a reference clock and an input data stream from an external data source. The data stream includes an embedded clock in a multi-bit combined data and missing clock pattern. Two shift registers each have a bit capacity less than the number of bits of the multi-bit pattern. The registers comprise respectively **samplers** for the incoming **data** in response to alternate **phases** of the reference **clock** .

A decoder is coupled to the outputs of the registers for detecting in which one the missing clock pattern is contained for producing a

detect signal at the output of that register. A logic circuitry is responsive to the detect signal for passing data from the other of the registers to a data storing portion.

USE/ADVANTAGE - For data stream from disc. Does not require two **phase clock** generator and one shots. May be made in MOS **integrated circuit** . (5pp Dwg.No.1/2)

Abstract (Equivalent): US 4625321 A

The device includes a reprogrammable digital circuit for impressing an analog attenuation signal on a continuous wave noise signal. The signal is fed to the input of a receiver and since the digital circuitry can be reprogrammed with a known sequence to effect a desired analog attenuation, a receiver's performance can be monitored and evaluated when the attenuated signal or error signal is simultaneously received with information signals.

A desired time relationship between the information signals and the time varying attenuating **test** signal or **error** signal is maintained since both are slaved to a common standard The programmable time varying attenuator is programmable independent of the information signal source. (6pp Dwg.No 1/2)

Title Terms: DUAL; EDGE; CLOCK; ADDRESS; MARK; DETECT; GENERATE; SYNCHRONOUS; SIGNAL; CONTROL; DECODE; IDENTIFY; TWO; REGISTER; CONTAIN; DATA; CONTAIN; CLOCK

Index Terms/Additional Words: DISC

Derwent Class: T03; U22; W01

International Patent Class (Additional): G11B-020/14; H03K-005/00;

H03K-021/02; H03K-023/66; H03M-005/06; H04K-001/02; H04L-007/02

File Segment: EPI

Manual Codes (EPI/S-X): T03-A06C; T03-N01; U22-H; W01-A04; W01-A04X

41/9/32 (Item 32 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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004769757

WPI Acc No: 1986-273098/198642

XRPX Acc No: N86-203859

Monitor for correct address and start data in multiplex system - employs integrated checking circuit in receivers with monitor scanning address input

Patent Assignee: NISSAN MOTOR CO LTD (NSMO)

Inventor: ABE N; OKADA K

Number of Countries: 004 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 3609487	A	19861009	DE 3609487	A	19860320	198642 B
GB 2173678	A	19861015	GB 866490	A	19860317	198642
JP 61227444	A	19861009	JP 8568762	A	19850401	198647
DE 3609487	C	19880714				198828
GB 2173678	B	19881207				198849
US 4811015	A	19890307	US 86838551	A	19860311	198912

Priority Applications (No Type Date): JP 8568762 A 19850401

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

DE 3609487 A 24

Abstract (Basic): DE 3609487 C

In a time division multiplexed transmission system a number of transmitters (40) and receivers (50) are addressed by the output of a serial mode address impulse generator (10). These addresses are sent

over an address bus (20). On another bus (70) the selected transmitter and receiver can communicate when the addresses are received correctly.

In the receiver (50) there is a monitor (90) which scans the address input. If this has remained at either logic high or logic low for a predetermined time a fault alarm signal is generated. The circuit also supervises the start bits sent from the transmitter over the data bus (70) in the same manner.

ADVANTAGE - Supervision system operates rapidly and needs no large capacitors. (24pp Dwg.No.1/6)

Abstract (Equivalent): GB 2173678 B

A circuit comprising: (a) first means for generating a periodic pulse train signal and transmitting the periodic pulse train signal on a first path; (b) second means for providing a path for transmitting a data from a first station to a second station when the periodic pulse train signal from said first means is received via the first path and one of the series of addresses derived from the periodic pulse train signal accords with a predetermined address which corresponds to, at least, the second station; (c) third means for generating and outputting a first signal when no pulse from said first means is present in the first path for a predetermined interval of time; (d) fourth means for generating and outputting a second signal when no data from said second means is present, the address being according with the predetermined address; and (e) fifth means for producing an alarm in response to at least one of said first and second signals.

Abstract (Equivalent): US 4811015 A

The circuit detects an abnormal transmission state on a signal transmission line, the abnormal state being such that a short-circuit or open-circuiting occurs in the signal transmission line, applicable to a time-division multiplex transmission network system having an address clock line and a data transmission line. The circuit includes a first latch circuit, which is set by a trailing edge of a data receivable interval specification pulse to a state indicating no presence of the specification pulse.

The specification pulse is derived from an address coincidence circuit constituting one data receiver of the network system. The first latch circuit latches the state of presence or absence of the specification pulse on a trailing edge of a start bit constituting data to be received.

USE/ADVANTAGE - Short detection time. Requires no capacitor of large capacity. Facilitates integration of whole circuit when applied to multichannel time-division data transmission network. (9pp)

Title Terms: MONITOR; CORRECT; ADDRESS; START; DATA; MULTIPLEX; SYSTEM;

EMPLOY; INTEGRATE; CHECK; CIRCUIT; RECEIVE; MONITOR; SCAN; ADDRESS; INPUT

Index Terms/Additional Words: TIME; DIVIDE

Derwent Class: W01; W05

International Patent Class (Additional): H01L-005/22; H04J-003/14;

H04L-001/24; H04L-005/22; H04L-011/00; H04Q-009/00

File Segment: EPI

Manual Codes (EPI/S-X): W01-A01 ; W01-A03; W05-D02; W05-D05

41/9/33 (Item 33 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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004261486

WPI Acc No: 1985-088364/198515

XRPX Acc No: N85-066118

Computer system with error correction using redundant memory arrays - counts occurrences of correctable errors detected by checking

arrangement and has system to substitute redundant array for faulty array

Patent Assignee: IBM CORP (IBM)

Inventor: SINGH S; SINGH V P

Number of Countries: 004 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 136443	A	19850410	EP 84108714	A	19840724	198515 B
US 4584681	A	19860422	US 83528769	A	19830902	198619
EP 136443	B	19910529				199122
DE 3484636	G	19910704				199128

Priority Applications (No Type Date): US 83528769 A 19830902

Cited Patents: A3...8735; EP 82981; No-SR.Pub; US 3999051; US 4209846; US 4375664; WO 8302164

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 136443 A E 20

Designated States (Regional): DE FR GB

EP 136443 B

Designated States (Regional): DE FR GB

Abstract (Basic): EP 136443 A

Thirty-six cards each store four bits of a 144-bit codeword having 16 **error** correction code **checking** bits in a triple **error detection** -double **error** correction code. The addressing of the cards is such that a **chip** row address enables only one of sixty-four **chips** in each of 144 bit array columns of the memory. Either one of two redundant array **chips** on a card may be substituted for any one of the 256 **chips** on a card. The substitution is effected in response to the counter which receives an input every time that a non-zero **detector** indicates that the **error** syndrome **bits** output by the syndrome generator are not all zero.

If the count exceeds a given value, the **chip** bill testing appts. is prompted to check the memory for a bad **chip**. If a bad **chip** is present then the appropriate address is passed by spare replacement logic control function to a register to substitute a redundant **chip** for the faulty **chip**.

ADVANTAGE - Minimum number of redundant memory **chips** is provided but **chip** replacement is effected with minimal or zero down-time.

0/8

Abstract (Equivalent): EP 136443 B

A computer system having a memory (32) protected by an **error checking** arrangement (30, 36, 44) in which data is stored in multi-bit position code words with different bit positions on different arrays (12) with spare array substitution means (16, 18, 20, 42) for substituting a spare array (16) for a faulty array (12), characterised by: counter means (38) for counting the number of occurrences of non-zero syndrome signals of a syndrome generator (30) of said **error checking** arrangement (36), said counter means being reset to zero at regular **time intervals** or upon reaching a threshold count, test means (40) for testing the memory for bad arrays by means of said **error checking** arrangement when the count in the counter exceeds that threshold count; and spare replacement logic means (42) controlled by said **test** means and by **error location** logic means (44) of said **error checking** arrangement. (17pp)

Abstract (Equivalent): US 4584681 A

Spare **chips** are used together with a replacement algorithm to replace **chips** in a memory array when failure is generally more extensive than unrelated cell fails in the memory **chips**. That is, substitution will be made if an error condition is a result of the

failure of a whole **chip** (**chip** -kill), a segment of a **chip** (island-kill), a column of bits of a **chip** or a row of bits of a **chip**, but will not be performed when it is due to a single failed cell.

The replacement of a **chip** with a **chip** -kill or with an island-kill is done on the fly and involves only a row of the memory **chips** or elements leaving other elements of the memory unaffected by the replacement.

ADVANTAGE - Down time is negligible. (13pp)t

Title Terms: COMPUTER; SYSTEM; ERROR; CORRECT; REDUNDANT; MEMORY; ARRAY; COUNT; OCCUR; CORRECT; ERROR; DETECT; CHECK; ARRANGE; SYSTEM; SUBSTITUTE; REDUNDANT; ARRAY; FAULT; ARRAY

Derwent Class: T01

International Patent Class (Additional): G01R-031/28; G06F-011/20

File Segment: EPI

Manual Codes (EPI/S-X): T01-G03; T01-H

41/9/34 (Item 34 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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003941233

WPI Acc No: 1984-086777/198414

XRFX Acc No: N84-064718

Communication channel pulse code sequence analyser - uses operative memory prior fed with clocking frequency which replaces HF clocking interval counter

Patent Assignee: KATSMAN V V (KATS-I)

Inventor: KATSMAN V V

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
SU 1023655	A	19830615	SU 3381799	A	19820108	198414 B

Priority Applications (No Type Date): SU 3381799 A 19820108

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
SU 1023655	A	3		

Abstract (Basic): SU 1023655 A

Analyser can be used to check digital **microcircuits**, cables and optical fibre communication lines. It operates in two modes, determining the probability of error occurrence k or fixing the number of errors in a given **time interval**.

Error detector sets the structural disruption of the initial sequence and produces an error signal to the error counter (7) input. Calculator (5) writes the counter indication which is divided by the timing frequency written in operative memory (3) and by a value in seconds shown on the electronic timer (8).

To simplify the construction, control unit is made like the operative memory and the calculator has a fixed dot digit setting. The synchronising unit (6) error counter (7) timer (8) and calculator (5) feed the corresp. control units. Bul.22/15.6.83.

Dwg.1/1

Title Terms: COMMUNICATE; CHANNEL; PULSE; CODE; SEQUENCE; ANALYSE; OPERATE; MEMORY; PRIOR; FEED; CLOCK; FREQUENCY; REPLACE; HF; CLOCK; INTERVAL; COUNTER

Derwent Class: S01; T01; W01; W02

International Patent Class (Additional): H03K-013/22

File Segment: EPI

Manual Codes (EPI/S-X): S01-G01A; T01-G02; **W01-A01** ; W02-C04; W02-C05

41/9/35 (Item 35 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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003722109

WPI Acc No: 1983-718301/198330

Related WPI Acc No: 1984-178129; 1984-178130; 1984-208446; 1984-226524;
1984-226525; 1984-226526; 1985-211303; 1989-101011

XRPX Acc No: N83-128496

**Audio-visual quality monitoring method for e.g. video disc - comparing
signature of input signal with signature of output and automatically
indicating out-of-tolerance condition**

Patent Assignee: DISCOVISION ASSOC (MCAC)

Inventor: EFRON E; KIM Y B; MCPHERSON J O

Number of Countries: 018 Number of Patents: 024

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 83686	A	19830720	EP 82108473	A	19820914	198330 B
JP 58120173	A	19830716				198334
US 4455634	A	19840619	US 82429347	A	19820930	198427
US 4524444	A	19850618	US 82429351	A	19820930	198527
US 4598324	A	19860701	US 82429350	A	19820930	198629
EP 83686	B	19860723				198630
DE 3272153	G	19860828				198636
US 4682246	A	19870721	US 82429349	A	19820930	198731
DE 3276896	G	19870903				198736
DE 3276995	G	19870917				198738
DE 3277281	G	19871015				198742
DE 3277997	G	19880218				198808
US 4746991	A	19880524	US 82339011	A	19820112	198823
US 4755884	A	19880705	US 86818572	A	19860113	198829
US 4764915	A	19880816	US 84625261	A	19840627	198835
DE 3279010	G	19881013				198842
KR 8802651	B	19881208				198930
KR 8802653	B	19881208				198930
KR 8802665	B	19881217				198930
KR 8802666	B	19881217				198930
KR 8802667	B	19881217				198930
US 5001568	A	19910319	US 82430902	A	19820930	199114
US 5126990	A	19920630	US 82339011	A	19820112	199229
			US 82429348	A	19820930	
JP 7078423	A	19950320	JP 82227895	A	19821228	199520
			JP 92333067	A	19821228	

Priority Applications (No Type Date): US 82339011 A 19820112; US 82429347 A
19820930; US 82429351 A 19820930

Cited Patents: DE 1084751; DE 1159010; DE 2049259; DE 2827422; US 3225135

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 83686 A E 82

Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE

EP 83686 B E

Designated States (Regional): AT BE CH DE FR GB IT LI LU NL SE

US 5126990 A 45 G11B-027/30 Div ex application US 82339011

Div ex patent US 4746991

JP 7078423 A 50 G11B-020/18 Div ex application JP 82227895

Abstract (Basic): EP 83686 A

The method evaluates the quality of audio and/or video transfer characteristics of a device which contains the information or through which the information passes. This involves measuring selected parameters of selected parts of an input signal. The input signal is fed to the unit under test and then the parameters of the output signal contained are measured. The parameters of the input and output signals are then compared.

A 'signature' is created for the unit under test. Subsequent analysis of the unit as it progresses along a production line or of a copy made on the same or alternate recording medium results in a second signature. The two signatures are compared to show the quality of the signal handling or transfer characteristics of the unit. The units to be evaluated may be tapes, discs, audio records, electronic storage and electronic circuits ranging from simple **integrated circuits** to macrosize amplifier **printed circuit** boards.

Abstract (Equivalent): EP 83686 B

A method of evaluating recording characteristics of a recording medium, comprising the steps of recording a timed sequence of test signals on a recording medium, retrieving the recorded test signals from the recording medium to recover a corresponding timed sequence of played back test signals, and analysing the retrieved test signals by comparing the retrieved signals against test standards, characterised in that: said recording step includes recording a plurality of separate and distinct audio test signals on said medium in a timed sequence of discrete audio test signal segments, said recording step including the step of spacing said recording segments such that the **time interval** between the start of each of said segments and the start of the next segment in sequence corresponds to an integer multiple of the duration of a frame of a standard video signal; and said analysing step includes correlating test signal deviation characteristics of each analysed played back signal segment with test signal deviation characteristics associated with the corresponding test signal segment used in said recording step. (44pp)

Abstract (Equivalent): US 5126990 A

The method involves unit evaluation which includes establishing an input signal of known content, measuring selected parameters of selected parts of the input signal, feeding the input signal to the unit under test, measuring the parameters of parts of the output signal from the unit corresponding to the same selected parts of the input signal, and comparing the selected parameters of the input signal with the corresponding parameters of the output signal.

Whether monitoring the quality of the signal transfer characteristics of a throughput device, a magnetic tape containing program material, or a video disc, master disc or replica, a 'signature' is created for the unit under test, and subsequent analysis of the unit as it progresses along a production line or of a copy made on the same or alternate recording medium results in a second 'signature' which is compared against the first signature to make a determination of the quality of the signal handling or transfer characteristics of the unit.

ADVANTAGE - Out-of-tolerance conditions are automatically detected, thereby eliminating subjectivity and providing consistency in quality level of device testing. (Dwg.3/27)

US 5001568 A

The apparatus receives a sequence of separate analog electrical signal segments at a real time sequence rate. Each segment contains at least one audio test signal at a real time data rate. A storage device coupled to the receiver accumulates the signal segments received in real times.

A controller coupled to the storage device sequentially releases the accumulated signal segments from the storage device at a sequence

rate slower than the real time sequence rate while maintaining the audio test signals at the real time data rate. A signal analyser is coupled to the storage device for receiving the released signal segments at the slower sequence rate and performing measurements on the audio test signal of each the segment.

USE - For analysing prescribed parameters of analog electrical signal. (44pp)nUS 4764915 A

The multiplexer comprises a number of audio channel test signal sources each having a test signal output that is unique as compared with other test signal outputs and a controller for enabling each of the test signal sources in sequential order. The outputs of the sources are combined to produce a serial sequence of audio channel test signals. A select-position register stores the position addresses of two reference positions on the storage member. A comparator has two inputs and a compare output.

A recorder reads program location information contained on the storage member and records the serial sequence of audio channel test signals onto the information storage member. A present position detector is connected to the output of the recorder for reading the program location information and outputting a present position address.

ADVANTAGE - Eliminates subjectivity and provides consistency in quality level of device testing. (45pp)c

US 4755884 A

In the method a predetermined picture frame number is established at which video evaluation of the audio portion of the program is to commence. The audio and video portions of the recorded audio-video program are recovered, and the picture frame code numbers are extracted from the video portion. The extracted picture frame numbers from the recovered video portion are then compared with the predetermined picture frame number, and audio evaluation of the audio portion of the program commences upon coincidence of the detected picture frame number and the predetermined picture number.

Evaluation is effected by measuring predetermined picture number. Evaluation is effected by measuring predetermined audio characteristics of the recovered audio portion and comparing the measured characteristics with corresponding audio reference characteristics. (45pp);

US 4746991 A

The method comprises the steps of recording a timed sequence of separate analog audio test signals onto each of the number of audio channels in a commonly times sequence in lead-in portions before, and lead-out portions after, prerecorded information on channels of the recording medium. The test signals are reproduced from the recording medium to produce a corresponding timed sequence of reproduced test signals from each of the audio channels.

The reproduced test signals of one of the of audio channels is compared with the reproduced test signals of another of the audio channels to produce comparison data. The comparison data is compared with test standards correlated with the comparison data.

ADVANTAGE - Out of tolerance conditions can to automatically detected. (45pp)i

US 4682246 A

The method of analysing the signal transferring characteristics of a video signal processing unit comprises the steps of: establishing an input video test signal of known content and measuring selected parameters of selected parts of the video input test signal. The video input test signal is fed to the signal processing unit.

The parameters of parts of the output from the signal processing unit are measured corresponding to the selected parts of the input signal. The selected parameters of the input signal are compared with

the corresponding parameters of the output signal.

ADVANTAGE - Eliminates subjectivity and provides consistency in quality. (45pp)i

US 4598324 A

A predetermined picture frame number at which video evaluation of the audio portion of the program is to commence is initially established. The audio and video portions of the recorded audio-video program are recovered, and the picture frame code numbers are extracted from the video portion. The numbers are then compared with the predetermined picture frame number, and evaluation of the audio portion of the program commences upon coincidence of the detected picture frame number and the predetermined picture number.

Evaluation is effected by measuring predetermined characteristics of the recovered audio portion and comparing the measured characteristics with corresponding reference characteristics. The measured audio characteristics of a storage member are stored in a memory device and used as a 'signature' for comparison with measured audio characteristics of a second storage member. (45pp)k

US 4524444 A

Unit evaluation is accomplished by establishing an input signal of known content, measuring selected parameters of selected parts of the input signal, feeding the input signal to the unit under test, measuring the parameters of parts of the output signal from the unit under test corresponding to the same selected parts of the input signal, and comparing the selected parameters of the input signal with the corresponding parameters of the output signal.

Whether monitoring the quality of the signal transfer characteristics of a throughput device, a magnetic tape containing program material, or a video disc, master disc or replica, a 'signature' is created for the unit under test, and subsequent analysis of the unit as it progresses along a production line or of a copy made on the same or alternate recording medium results in a second 'signature' which is compared against the first signature to make a determination as to the quality of the signal handling or transfer characteristics of the unit. The system comprises a central controller with its peripheral memory, keyboard, and readout devices, an audio test subsystem, a video test subsystem, and a data evaluation subsystem.

ADVANTAGE - Out-of-tolerance conditions can be automatically detected, thereby eliminating subjectivity and providing consistency in the quality level of device testing. (46pp)V

US 4455634 A

The method establishes the characteristics of a program of recorded information previously recorded on two channels of a recording medium. The method **samples** the audio waveform amplitude of audio information contained on each channel of the recorded program. The amplitudes of the information **sampled** from one channel, are compared with the amplitudes of information occurring simultaneously with that **sampled** from the other channel.

The number of times that the amplitudes of the **samples** from the two channels are within a prescribed percentage tolerance of one another, are counted. This provides information regarding whether or not the signals on the two channels are similar in informational content.1

Title Terms: AUDIO; VISUAL; QUALITY; MONITOR; METHOD; VIDEO; DISC; COMPARE; SIGNATURE; INPUT; SIGNAL; SIGNATURE; OUTPUT; AUTOMATIC; INDICATE; TOLERANCE; CONDITION

Derwent Class: S01; T03; W04

International Patent Class (Main): G11B-020/18 ; G11B-027/30

International Patent Class (Additional): G01R-031/00; G11B-005/84; G11B-007/24; G11B-011/00; G11B-023/18; G11B-027/36; H04N-005/13;

H04N-017/06
File Segment: EPI
Manual Codes (EPI/S-X): S01-G01; W04-F; W04-G; W04-J

41/9/36 (Item 36 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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003344089

WPI Acc No: 1982-K2108E/198231

**Modular structure for PCM distributed-control and diagnostic network -
uses integrated switching matrices with microprocessor-compatible
asynchronous control, allowing fault location, diagnosis,
reconfiguration**

Patent Assignee: CSELT CENT STUDI LA (CSEL); CSELT CENT STUDI LAB TELECOM
SPA (CSEL)

Inventor: BELFORTE P; BONDONNO M; GARETTI E; GUASCHINO G; PILATI L

Number of Countries: 015 Number of Patents: 009

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 56600	A	19820728	EP 82100149	A	19820111	198231 B
JP 57138292	A	19820826				198240
BR 8200049	A	19821026				198248
DK 8200134	A	19821213				198303
US 4473900	A	19840925	US 82339101	A	19820113	198441
EP 56600	B	19841128				198448
DE 3261306	G	19850110				198503
CA 1195760	A	19851022				198547
IT 1143268	B	19861022				198830

Priority Applications (No Type Date): IT 8167036 A 19810115

Cited Patents: 3.Jnl.Ref; EP 27226; EP 3448; EP 34776; EP 39134; EP 39948;
FR 2382819; GB 2029671; EP 26931; US 4093827

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 56600 A E 33

Designated States (Regional): AT BE CH DE FR GB LI NL SE

EP 56600 B E

Designated States (Regional): AT BE CH DE FR GB LI NL SE

Abstract (Basic): EP 56600 A

The PCM-switched network has a number of **time stages** forming part of a centralised-control exchange. It comprises modular connections having integrated switching matrices with a microprocessor-compatible asynchronous control system. **Integrated support circuits** are provided for diagnosis and a microprocessor forms the lowest level of a three-level hierarchical control network.

For five **time stages**, the modular connecting units are diversified in a number of peripheral connections, folded from the building standpoint, comprising the first and fifth stages, and a number of central connecting units folded similarly for the **second** and fourth **stages**. The third stage consists of a number of unfolded central connecting units. The system allows **diagnosis, fault location**, and reconfiguration functions to be claimed out by the single building blocks, without artificial test traffic being generated.

Abstract (Equivalent): EP 56600 B

The system includes modular switching units divided into groups of peripheral units and comprising the first and large **time stage** of

the network. Central switching units folded from the building standpoint comprise the second and last but one **time stages** and unfolded units comprise the intermediate stages. Each peripheral unit of the folded and unfolded units are contained in a single pcb which can be extracted and replaced.

The modular switching units comprise integrated switching matrices equipped with a microprocessor-compatible async. control system. A further microprocessor forms the lowest level of a multilevel hierarchical control network. Distributed diagnosis is performed at the level of each modular structural element by the **integrated support circuits** in conjunction with the microprocessor. (21pp)

Abstract (Equivalent): US 4473900 A

A five-stage PCM switching network is divided into a set of outer modular units each including a first-stage and a fifth-stage matrix, a set of inner modular units each including a **second - stage** and a fourth-stage matrix, and a set of central modular units each including a pair of third-stage matrices. Each modular unit is provided with an individual base-level microprocessor controlling the switching of its matrices and the checking of their performance with the aid of ancillary equipment including transceivers sending back outgoing **signals** and **samplers** delivering bytes from corresponding time slots at opposite ends of an established signal path to a comparator in the associated microprocessor.

Each set is divided into several subsets provided with respective intermediate-level microprocessors which control their base-level microprocessor.

USE/ADVANTAGE - For automatic telephone exchange number of lines affected by partial deactivation is minimised. (14pp)

Title Terms: MODULE; STRUCTURE; PCM; DISTRIBUTE; CONTROL; DIAGNOSE; NETWORK ; INTEGRATE; SWITCH; MATRIX; MICROPROCESSOR; COMPATIBLE; ASYNCHRONOUS; CONTROL; ALLOW; FAULT; LOCATE; DIAGNOSE; RECONFIGURE

Derwent Class: W01

International Patent Class (Additional): G06F-011/00; H03K-013/01; H04J-003/00; H04Q-001/20; H04Q-003/54; H04Q-011/04

File Segment: EPI

Manual Codes (EPI/S-X): W01-B02A; W01-B07; W01-B08

? t41/9/38-42

41/9/38 (Item 38 from file: 347)

DIALOG(R)File 347:JAPIO

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06565826 **Image available**

DATA SYNCHRONOUS DEVICE, METHOD THEREFORE AND NONCONTACT IC CARD HAVING DATA SYNCHRONOUS DEVICE

PUB. NO.: 2000-151569 [JP 2000151569 A]

PUBLISHED: May 30, 2000 (20000530)

INVENTOR(s): TSUJII HITOSHI

APPLICANT(s): SONY CORP

APPL. NO.: 11-249428 [JP 99249428]

FILED: September 03, 1999 (19990903)

PRIORITY: 10-249896 [JP 98249896], JP (Japan), September 03, 1998 (19980903)

INTL CLASS: H04L-007/027; G06K-019/07

ABSTRACT

PROBLEM TO BE SOLVED: To enable data synchronization for sure waveform shape without being influenced by a jitter or a glitch with a simple structure by monitoring a position where an edge signal exists in accordance with a second timing signal and outputting a preset signal when

the position is in a **period** of a first **timing** signal or a **period** of a neighborhood of the signal.

SOLUTION: A start detection part 102 detects a first edge signal from the edge detection part 101 to be outputted after an input signal is supplied and generates a start signal for starting count operation of a counter 104 based on the signal. A synchronous **deviation detection** part 103 **detects** whether or not an edge of the input signal exists in a period in which the **input signal** is **sampled** when a count value of the counter 104 is a specified value. When it exists, it is regarded that data synchronous deviation occurs, a synchronous **deviation detection** signal is outputted, this signal is transmitted to the counter 104 and the count value of the counter 104 is preset to a specified value.

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41/9/39 (Item 39 from file: 347)

DIALOG(R)File 347:JAPIO

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06504974 **Image available**

SEMICONDUCTOR MEMORY DEVICE WITH ON-CHIP ERROR CORRECTING CIRCUIT AND ERROR CORRECTING METHOD

PUB. NO.: 2000-090691 [JP 2000090691 A]

PUBLISHED: March 31, 2000 (20000331)

INVENTOR(s): LEE JIN-YUB

APPLICANT(s): SAMSUNG ELECTRONICS CO LTD

APPL. NO.: 11-224644 [JP 99224644]

FILED: August 06, 1999 (19990806)

PRIORITY: 9832236 [KR 9832236], KR (Korea) Republic of, August 07, 1998 (19980807)

INTL CLASS: G11C-029/00; G06F-011/10; G06F-012/16; G11C-016/04

ABSTRACT

PROBLEM TO BE SOLVED: To improve an access time by simultaneously receiving data and check bits in two groups, generating syndrome bits in corresponding two rows in the data and the check bits in the two groups respectively and correcting **errors** in data **bits** in the two groups respectively in response to the syndrome bits in the two rows.

SOLUTION: An **error detector** 202 for the **error** correcting circuit 200-bottom receives nine syndrome bits from a syndrome generator 201 and outputs a signal displaying the presence of an error, and an error corrector 203 successively receives 256 data bits from a first sense amplifier 140-bottom through a switch circuit 161-2 during a **second cycle**, and corrects one **error bit** in the 256 data bits in response to a signal from the **error detector** 202. An **error** correcting circuit 200-top executes the same functions as the components of the error correcting circuit 200-bottom.

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41/9/40 (Item 40 from file: 347)

DIALOG(R)File 347:JAPIO

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05851274 **Image available**

SIGNAL PROCESSOR FOR DISK

PUB. NO.: 10-134374 [JP 10134374 A]
PUBLISHED: May 22, 1998 (19980522)
INVENTOR(s): FUKUDA MITSUYOSHI
APPLICANT(s): SANYO ELECTRIC CO LTD [000188] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-290716 [JP 96290716]
FILED: October 31, 1996 (19961031)
INTL CLASS: [6] G11B-007/09; **G11B-020/18** ; **G11B-020/18**
JAPIO CLASS: 42.5 (ELECTRONICS -- Equipment)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce the circuit scale of hardware and to improve software efficiency and servo characteristic at the time of CDROM reproduction, in an **LSI** with three functions loaded, namely, digital servo processing, **error detection** /correction processing, and audio signal processing.

SOLUTION: A CPU bus 23 is connected commonly with an **error detecting** and correcting part 21 in an exclusive hardware structure for performing **error detecting** and correcting processing, with a servo part 20 consisting of an AD converter 200 and a DA converter 201 for servo control input and output, and with an audio part 22 consisting of a FIFO register 34 for storing audio data and a DA converter 221 for outputting an audio signal; a CPU 24 carries out a digital servo processing and an audio **signal** processing within a **sampling** period t repeatedly at every $t/2$ at the time of reproducing an audio CD, and carries out a digital servo processing twice within the **sampling period** t at the **time** of reproducing a CD-ROM.

41/9/41 (Item 41 from file: 347)

DIALOG(R) File 347:JAPIO

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05506402 **Image available**
RAKE SYSTEM SPREAD SPECTRUM RECEIVER

PUB. NO.: 09-121202 [JP 9121202 A]
PUBLISHED: May 06, 1997 (19970506)
INVENTOR(s): TOMINAGA HIDEO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-277416 [JP 95277416]
FILED: October 25, 1995 (19951025)
INTL CLASS: [6] H04J-013/00; H04L-007/00; H04L-012/00
JAPIO CLASS: 44.2 (COMMUNICATION -- Transmission Systems); 44.3 (COMMUNICATION -- Telegraphy)

ABSTRACT

PROBLEM TO BE SOLVED: To realize a correct **data** reproduction without **sampling** the changed point of a reception base band **signal** by the **sampling** frequency of a **chip** rate by performing the synchronizing acquisition and the synchronizing holding by a time window so as not to sample the changed point of the reception base band signal.

SOLUTION: A block **phase** control type **time** window control part 8 performs the synchronizing acquisition and the synchronizing holding by a time window so as not to sample the changed points of a reception base band signal I and a reception base band signal Q in matched filters 3 and 4, and

outputs the time window signal showing the time window. Namely, deterioration in the samplings of the changed points of the base band signals I and Q and the peak value of the envelope information signal due to the step-out in the synchronizing holding state are detected, and in the **detection** of **deterioration** the phase of an N frequency divider is shifted less than when the **deterioration** is not **detected**. Thus, the **detection** of the **degraded** peak value can be prevented in advance and an exact data reproduction can be realized.

41/9/42 (Item 42 from file: 347)

DIALOG(R)File 347:JAPIO

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04466890 **Image available**

MEMORY CONTROLLER

PUB. NO.: 06-110790 [JP 6110790 A]

PUBLISHED: April 22, 1994 (19940422)

INVENTOR(s): CHIYOU KOKUSEI

APPLICANT(s): TOKYO ELECTRIC CO LTD [000356] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 04-256956 [JP 92256956]

FILED: September 25, 1992 (19920925)

INTL CLASS: [5] G06F-012/16; G06F-011/10

JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)

JAPIO KEYWORD:R129 (ELECTRONIC MATERIALS -- Super High Density **Integrated Circuits , LSI & GS**

JOURNAL: Section: P, Section No. 1774, Vol. 18, No. 391, Pg. 127, July 21, 1994 (19940721)

ABSTRACT

PURPOSE: To attain the control of a memory using an **ECC** (**error** correction code) **bit** through the use of a memory control part for parity on the market.

CONSTITUTION: When a memory control signal monitoring circuit 71 monitors a memory control signal from the memory control part 3 for parity to detect the access cycle of DRAM 2', a clock control circuit 74 changes the **cycle** of a **clock** signal provided for the memory control part 3 for parity and an **ECC** circuit 8 is actuated. In addition to it, the memory control signal generated by a memory control signal generation circuit 73 is provided for DRAM 2' to access-control DRAM 2' using the **ECC** bit.

File 348:EUROPEAN PATENTS 1978-2003/Oct W01

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File 349:PCT FULLTEXT 1979-2002/UB=20031009,UT=20031002

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? ds

Set	Items	Description
S1	961388	TIME OR TIMING OR TIMER? ? OR CLOCK??? ? OR TEMPORAL
S2	1142366	MINUTE? ? OR SECOND? ?
S3	418023	S1:S2(3N) (INTERVAL? ? OR PHASE OR PHASES OR ZONE OR ZONES - OR PERIOD? ? OR CYCLE OR CYCLES OR SECTOR? ? OR DURATION? OR - STAGE OR STAGES)
S4	337050	SAMPLE? OR SAMPLING?
S5	5756	ECC OR EDAC
S6	919797	INVALID? OR MISTAK? OR FAIL? OR PROBLEM? OR FAULT? OR DEFE- CT? OR DEFICIEN? OR ABNORMA? OR FLAW? OR ABERRA? OR MALFUNCTI- ON?
S7	418659	INOPERA? OR UNUSUAL OR DYSFUNCTION? OR DISFUNCTION? OR BUG? ? OR DETERIORAT? OR ATYPICAL? OR ERROR? ? OR DEVIA? OR IRREG- ULAR? OR CORRUPT?
S8	311425	IMBALANC? OR EXCEPTION? ? OR DISTORT? OR DEGRAD? OR DISPAR- AT?
S9	111038	S6:S8(3N) (DETECT? OR DISCERN? OR FIND??? ? OR FOUND OR UNC- OVER? OR UN()COVER? OR CHECK? OR CHEQU? OR DIAGNOS? OR LOOK??? ? OR SEEK??? ?)
S10	68850	S6:S8(3N) (PROBE? ? OR PROBING OR SEARCH? OR ESTIMAT? OR EV- ALUAT? OR SURVEY? OR ANALYS? OR ANALYZ? OR ANALYT? OR ASSESS? OR EXAMIN? OR LOCAT? OR REVIEW? OR IDENTIFIC? OR IDENTIFIE? OR IDENTIFY?)
S11	24680	S6:S8(3N) (DISCRIMINAT? OR SCRUTIN? OR DIFFERENTIAT? OR SCR- EEN? OR PINPOINT? OR PIN()POINT??? ? OR RECOGNIT? OR RECOGNIS? OR RECOGNIZ?)
S12	53216	S6:S8(3N) (ASCERTAIN? OR INSPECT? OR DISTINGUISH? OR MONITO- R? OR TRACK? OR TROUBLESHOOT? OR TROUBLE()SHOOT? OR SCAN OR S- CANS OR SCANN??? ? OR TEST??? ?)
S13	952	SELFTEST? OR SELFDIAGNOS? OR BIST
S14	254289	IC OR ICS OR INTEGRAT?? ?(1W) (CIRCUIT? OR OPTOELECTRONIC? - OR OPTO()ELECTRONIC? ?) OR CHIP OR CHIPS OR MICROCIRCUIT? OR - MICROELECTRONIC? ?
S15	43051	MICRO() (CIRCUIT? OR ELECTRONIC? ?) OR PRINTED(1W)CIRCUIT? - OR MICROCHIP?
S16	63361	ASI OR ASIC OR VLSI OR VLSIC OR ULSI OR ULSIC OR VHSI OR V- HSIC OR SOI OR SOIC OR MSI OR MSIC OR LSI OR LSIC
S17	6559	S3(20N) (S5 OR S9:S13)
S18	296	S17(S) S14:S16
S19	9	S18/TI, AB
S20	60	S18(S) S4
S21	9	S20/TI, AB, CM
S22	25222	S3(10N) S4
S23	24	S18(S) S22
S24	56401	S4(3N) (DATA OR INPUT? OR SIGNAL? ? OR TRAFFIC? OR DATASTRE- AM? OR STREAM?)
S25	32398	BER OR BERT OR (BIT OR BITS OR MULTIBIT? ?) (2N)ERROR?
S26	35	S18(S) S24
S27	34	S18(S) S25
S28	5102	IC='H04L-001'
S29	3	S18 AND S28
S30	38	S19 OR S21 OR S23 OR S29
S31	10	S26:S27 AND S17/TI, AB, CM
S32	40	S30:S31
S33	40	IDPAT (sorted in duplicate/non-duplicate order)

S34 40 IDPAT (primary/non-duplicate records only)
? t34/5,k/5,7

34/5,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01058607

Method for mounting flip-chip semiconductor devices
Verfahren zur Montage von Flip-Chip-Halbleiterbauelementen
Procede de montage de dispositifs semiconducteurs du type flip-chip
PATENT ASSIGNEE:

SHIN-ETSU CHEMICAL CO., LTD., (235614), 6-1, Ohtemachi 2-chome,
Chiyoda-ku Tokyo, (JP), (Applicant designated States: all)

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Arai, Kazuhiro, Silicone-Electr. Materials Lab., Shin-Etsu Ch.Co.Ltd.,
1-10 Oaza Hitomi, Matsuida-machi, Usui-gun, Gunma-ken, (JP)

LEGAL REPRESENTATIVE:

Stuart, Ian Alexander et al (50492), MEWBURN ELLIS York House 23 Kingsway
, London WC2B 6HP, (GB)

PATENT (CC, No, Kind, Date): EP 933809 A2 990804 (Basic)
EP 933809 A3 000329

APPLICATION (CC, No, Date): EP 99300697 990129;

PRIORITY (CC, No, Date): JP 9835453 980202

DESIGNATED STATES: DE; FR; GB

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: H01L-021/56

ABSTRACT EP 933809 A2

When a semiconductor chip is mounted on a circuit substrate, the space therebetween can be rapidly sealed with a resin encapsulant by transfer molding an encapsulating resin composition in molten state and under pressure into the space and heat curing the composition thereat. The composition contains (a) an epoxy resin, (b) a curing agent, and (c) an inorganic filler having a maximum particle size of up to 24 (mu)m and has a melt viscosity of up to 200 poises at the molding temperature. Then encapsulation can be completed within a very short cycle without allowing the filler to settle. Semiconductor devices are manufactured to high reliability.

ABSTRACT WORD COUNT: 107

NOTE:

Figure number on first page: 3

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination: 000823 A2 Date of request for examination: 20000626
Search Report: 20000329 A3 Separate publication of the search report
Application: 990804 A2 Published application (Alwith Search Report
;A2without Search Report)

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9931	169
SPEC A	(English)	9931	3555
Total word count - document A			3724
Total word count - document B			0
Total word count - documents A + B			3724

...SPECIFICATION were placed in a pressure cooker at 121(degree)C and 2.1 atmospheres. The **samples** were taken out at predetermined **time**

intervals , and the separation between the chip surface and the resin was observed by an ultrasonic flaw detector . The results are shown in Table 4.

Japanese Patent Application No. 035453/1998 is incorporated...

34/5,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00823895

MITIGATION OF MULTIPATH EFFECTS IN GLOBAL POSITIONING SYSTEM RECEIVERS
VERRINGERUNG DES MEHRWEGEFFEKTS IN GPS-EMPFANGERN
ATTENUATION DES EFFETS DES TRAJETS MULTIPLES DANS LES RECEPTEURS DE SYSTEMES GPS

PATENT ASSIGNEE:

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INVENTOR:

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KEEGAN, Richard, Gerald, 5330 Halison Street, Torrance, CA 90503, (US)

HATCH, Ronald, Ray, 1142 Lakme Avenue, Wilmington, CA 90744, (US)

CAHN, Charles, Robert, 225 20th Street, Manhattan Beach, CA 90266, (US)

LEGAL REPRESENTATIVE:

Kaminski, Susanne et al (73524), Buchel, Kaminski & Partner Austrasse 79, 9490 Vaduz, (LI)

PATENT (CC, No, Kind, Date): EP 830616 A1 980325 (Basic)

EP 830616 B1 021113

WO 96037789 961128

APPLICATION (CC, No, Date): EP 96921225 960524; WO 96US7774 960524

PRIORITY (CC, No, Date): US 449215 950524

DESIGNATED STATES: CH; DE; FR; GB; IT; LI; NL; SE

INTERNATIONAL PATENT CLASS: G01S-001/04; H04B-001/707

CITED PATENTS (EP B): EP 552975 A; WO 87/01540 A; US 5347536 A

NOTE:

No A-document published by EPO

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination: 010328 A1 Date of dispatch of the first examination report: 20010212

Application: 970326 A1 International application (Art. 158(1))

Lapse: 030723 B1 Date of lapse of European Patent in a contracting state (Country, date): NL 20021113, SE 20030213,

Grant: 021113 B1 Granted patent

Change: 020717 A1 Legal representative(s) changed 20020529

Lapse: 030507 B1 Date of lapse of European Patent in a contracting state (Country, date): SE 20030213,

Application: 980325 A1 Published application (A1with Search Report ;A2without Search Report)

Examination: 980325 A1 Date of filing of request for examination: 971223

Change: 990804 A1 Representative (change)

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200246	1095
CLAIMS B	(German)	200246	1040
CLAIMS B	(French)	200246	1248

SPEC B	(English)	200246	24656
Total word count - document A			0
Total word count - document B			28039
Total word count - documents A + B			28039

...SPECIFICATION within a C/A code chip and 4 within a P code chip. With this **clock**, the **phase** MMW **samplers** of FIGS. 30B and 30D could be as narrow as 0.025 (1/40) of a C/A code **chip**. Therefore, the signal energy processed during either interval A or interval B is 0.025 times the energy processed during an entire C/A code **chip**, which results in a signal-to-noise (S/N) power reduction of 16 dB.
Fortunately...

34/5,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00369499

A sampled data phase locking system.

System zur Phasenverriegelung abgetasteter Daten.

Systeme pour le verrouillage de phase des donnees echantillonnees.

PATENT ASSIGNEE:

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Princeton New Jersey 08540, (US), (applicant designated states:
AT;DE;ES;FR;GB;IT)

INVENTOR:

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LEGAL REPRESENTATIVE:

Pratt, Richard Wilson et al (46454), London Patent Operation G.E.
Technical Services Co. Inc. Essex House 12/13 Essex Street, London WC2R
3AA, (GB)

PATENT (CC, No, Kind, Date): EP 361747 A2 900404 (Basic)
EP 361747 A3 900912
EP 361747 B1 940202

APPLICATION (CC, No, Date): EP 89309413 890915;

PRIORITY (CC, No, Date): US 249022 880926; US 324875 890317

DESIGNATED STATES: AT; DE; ES; FR; GB; IT

INTERNATIONAL PATENT CLASS: H04N-009/455;

ABSTRACT EP 361747 A2

A phase locking system for phase/frequency providing a sampling signal which is to be phase frequency locked to an applied signal includes a controllable oscillator (86) coupled to a sampling circuit (50-53) to produce samples of the applied signal representing substantially quadrature phase related components of the applied signal. An accumulator (54,58,60) respectively accumulates the quadrature phase components over predetermined intervals. A differencing circuit (62-70) successively forms the differences of one of the components from successive intervals. The differences are used (74,88-94,108) to generate a control signal to alter the signal generated by the controlled oscillator.

ABSTRACT WORD COUNT: 100

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 900404 A2 Published application (Alwith Search Report
;A2without Search Report)
Search Report: 900912 A3 Separate publication of the European or
International search report
Examination: 910220 A2 Date of filing of request for examination:
901217
Change: 920624 A2 Representative (change)
*Assignee: 920624 A2 Applicant (transfer of rights) (change): RCA
Thomson Licensing Corporation (944402) 2
Independence Way Princeton New Jersey 08540
(US) (applicant designated states:
AT;DE;ES;FR;GB;IT)
Examination: 920923 A2 Date of despatch of first examination report:
920810
Grant: 940202 B1 Granted patent
Oppn None: 950125 B1 No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	541

CLAIMS B	(German)	EPBBF1	501
CLAIMS B	(French)	EPBBF1	602
SPEC B	(English)	EPBBF1	5462
Total word count - document A			0
Total word count - document B			7106
Total word count - documents A + B			7106

...SPECIFICATION clock signal can be generated which is phase locked to the subcarrier frequency by a) **sampling** the burst component to **produce** substantially quadrature **phase** related **samples** of the burst signal; b) accumulating the respective quadrature samples; and c) generating a signal...

...in US-A-4,491,862 entitled "Color Television Receiver with At Least One Digital **Integrated Circuit** For Processing The Composite Color Signal", issued to Peter Flamm. The Flamm system includes an...

...accumulated R-Y and B-Y samples are coupled to a switching circuit. The R- Y accumulated **samples** are **applied** to a **value** limiter circuit, and the limited **samples** coupled to the switching circuit. The sign bits of the accumulated **samples** indicate whether the **phase** of the **clock** signal generated by the VCO is greater or less than + or - 90(degree) relative to...

...signal, and applied to the control input of the VCO to form a closed loop **phase** locked **clock** generator.

There are at least two shortcomings of the Flamm circuitry. Firstly the phase **detection** is a **function** of signal amplitude. The detection accuracy diminishes with smaller signal amplitude. Secondly, since phase detection...

34/5,K/12 (Item 12 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00365631

AFC apparatus.

AFC-Gerat.

Appareil AFC.

PATENT ASSIGNEE:

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., (216883), 1006, Oaza Kadoma, Kadoma-shi, Osaka, (JP), (applicant designated states: DE;FR;GB)

INVENTOR:

Omoto, Noriaki, 21-11, Kamihamuro-5-chome, Takatsuki-shi, (JP)

LEGAL REPRESENTATIVE:

Smith, Norman Ian et al (36041), F.J. CLEVELAND & COMPANY 40-43 Chancery Lane, London WC2A 1JQ, (GB)

PATENT (CC, No, Kind, Date): EP 344991 A2 891206 (Basic)
 EP 344991 A3 901031
 EP 344991 B1 931215

APPLICATION (CC, No, Date): EP 89305378 890526;

PRIORITY (CC, No, Date): JP 88131854 880530; JP 88307992 881206

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: H03J-007/06; H04N-005/50; H04N-007/04;

CITED PATENTS (EP A): US 4689685 A

CITED REFERENCES (EP A):

PATENT ABSTRACTS OF JAPAN vol. 5, no. 44 (E-50)(716) 24 March 1981,
 & JP-A-56 782 (SANYO DENKI K.K.) 07 January 1981,;

ABSTRACT EP 344991 A2

An AFC apparatus effectively used for a satellite broadcasting receiver and making up a tuning circuit of frequency synthesizer system using a phase-locked loop (PLL) is disclosed, in which a frequency error detector (4) for detecting an error of an output signal of a demodulator (3) from the central frequency comprises first and second comparators (8, 9) supplied with an output of the demodulator and reference voltages 12, 13), a first latch circuit (20) for latching an output of the first comparator by a key pulse, and a second latch circuit (21) for latching an output of the second comparator by a key pulse. A demodulation output is thus accurately held to realize an accurate data comparison even against a key pulse of a large duty factor.

ABSTRACT WORD COUNT: 131

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 891206 A2 Published application (A1with Search Report
;A2without Search Report)
Search Report: 901031 A3 Separate publication of the European or
International search report
Change: 901128 A2 Obligatory supplementary classification
(change)
Examination: 910206 A2 Date of filing of request for examination:
901206
Examination: 920916 A2 Date of despatch of first examination report:
920731
Grant: 931215 B1 Granted patent
Oppn None: 941207 B1 No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	338
CLAIMS B	(German)	EPBBF1	400
CLAIMS B	(French)	EPBBF1	517
SPEC B	(English)	EPBBF1	3939
Total word count - document A			0
Total word count - document B			5194
Total word count - documents A + B			5194

...SPECIFICATION off frequencies and for filtering said demodulation signal before being supplied to said first and **second** comparators, said cut-off frequencies being changeable to control a **time** constant of said **low** -pass filter according to presence or absence of said **key** pulse.

According to another aspect of the present invention, there is provided an AFC apparatus...

...supplied with a first reference voltage and an output of a demodulator through a low- **pass** filter having a control terminal for switching two type of cut-off frequency, a second...

34/5,K/13 (Item 13 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00276101

Predictive clock recovery circuit.

Pradiktive Taktwiedergewinnungsschaltung.

Circuit de recuperation d'horloge predictif.

PATENT ASSIGNEE:

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Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB;IT)

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Jeannot, Patrick, 173, Chemin de l'Hermitage, F-06610 La Gaude, (FR)
Lallemand, Eric, Villa "Le bois joli" Chemin des Chauvets, F-06610 La
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LEGAL REPRESENTATIVE:

Schuffenecker, Thierry (69981), Compagnie IBM France, Departement de
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PATENT (CC, No, Kind, Date): EP 312671 A1 890426 (Basic)
EP 312671 B1 930127
APPLICATION (CC, No, Date): EP 87480014 871019;
PRIORITY (CC, No, Date): EP 87480014 871019
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: H04L-007/02;
CITED PATENTS (EP A): WO 8504775 A; WO 8504775 A; EP 228021 A
CITED REFERENCES (EP A):
PATENT ABSTRACTS OF JAPAN, vol. 11, no. 4 (E-468) 2451 , 7th January
1987; & JP-A-61 179 630 (FUJITSU LTD) 12-08-1986;

ABSTRACT EP 312671 A1

Predictive clock extracting circuit which having means for determining the duration between two consecutive transitions of a multilevel digital signal, and means for generating a pulse SPL at half the said duration after a the transition following on two consecutive previous transitions. A phase locked oscillator (23) driven by said SPL pulse generates the extracted clock signal, in phase with pulse SPL and which coincides with the center of the eye intervals of said multilevel digital signal. The system includes a first counter N (20) which starts running in response to the detection of the first transition of the multilevel digital signal. The running stops when the second transition occurs, the result N(i) stored into the first counter N at second transition is therefore representative of the duration between the two consecutive first and second transitions. A divide by 2 circuit (21) divides the result N(i) stored into the first counter at second transition. The preferred embodiment of the invention also involves an an up/down counter which generates a second counter K that is expected to be representative of half the value of the first counter N(i). This second counter K is used to generate the extracted clock in phase with the middle of the eye intervals. Counter K is adaptively updated by incrementing its current value K(i) by a fixed factor or, on the contrary, by decrementing its current value K(i) by a fixed damping factor. A comparator comparing K(i) and N(i)/2 controls the update of the current value K(i) according the following rules. if the value K(i) is superior to N(i)/2 at the second transition, then the counter K is updated by decrementing its current value. Conversely, when N(i) is inferior to N(i)/2, then counter K is updated by incrementing its current value. In this way, the extracted clock which will be derived from counter K varies slowly and integrates sudden variations of the content of the first counter N. A counter P (22) initialized with the updated value K(i+1) of counter K starts running from K(i+1) to zero in response to the detection of the transition following on two said first and second transition and delivers a pulse SPL whenever its content reaches the value zero. The phase locked oscillator (23) controlled by the pulse SPL generates the extracted clock which is likely to coincide with the middle of the eye pattern.

ABSTRACT WORD COUNT: 402

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application: 890426 A1 Published application (A1with Search Report

;A2without Search Report)

Examination: 891004 A1 Date of filing of request for examination:
890809
Examination: 911016 A1 Date of despatch of first examination report:
910830
Grant: 930127 B1 Granted patent
Oppn None: 940119 B1 No opposition filed
Lapse: 991020 B1 Date of lapse of European Patent in a
contracting state (Country, date): IT
19930127,

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1365
CLAIMS B	(German)	EPBBF1	772
CLAIMS B	(French)	EPBBF1	838
SPEC B	(English)	EPBBF1	6009
Total word count - document A			0
Total word count - document B			8984
Total word count - documents A + B			8984

...SPECIFICATION a plurality of transition marker signal groups, each transition marker signal group being followed in **time** by a eye **interval** . To assure that the **sampling** time will occur at the "middle of the eye", this system uses a particular phase **error detection** circuit 400 (column 10, line 45 and following). This circuit 400 is designed for counting...circuitry for generating a sinusoidal signal, that will be difficult to integrate in a simple **chip** .

US patent 4,295,222 describes an arrangement for restituting the clock and for sampling...

34/5,K/15 (Item 15 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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01035593 **Image available**

PILOT FREQUENCY ACQUISITION BASED ON A WINDOW OF DATA SAMPLES
ACQUISITION DE FREQUENCE PILOTE BASEE SUR UNE FENETRE D'ECHANTILLONS DE
DONNEES

Patent Applicant/Assignee:

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Inventor(s):

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ROH Mark Charles, 8520 Costa Verda Boulevard, #3223, San Diego, CA 92122,
US,

PATEL Shimman, 9406 Galvin Avenue, San Diego, CA 92126, US,

Legal Representative:

WADSWORTH Philip R (et al) (agent), 5775 Morehouse Drive, San Diego, CA
92121, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200365673 A1 20030807 (WO 0365673)

Application: WO 2003US2906 20030131 (PCT/WO US0302906)

Priority Application: US 2002353479 20020131; US 2003356296 20030130

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU

CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP

KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO

RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW

(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PT SE SI
SK TR

(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: H04L-027/00

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 10929

English Abstract

Techniques to acquire the frequency of a signal instance based on a window of data samples covering a time period shorter than the time needed to achieve frequency lock. The window of data samples is initially captured and stored to a sample buffer. A segment of data samples is then retrieved from the sample buffer for processing. The retrieved data samples are rotated by a current frequency error estimate to provide frequency-translated data samples, which are further processed to provide one or more pilot symbols. An updated frequency error estimate for the frequency-translated data samples is then derived based on the pilot symbols using a frequency control loop. The window of data samples is processed for a number of iterations until frequency acquisition is achieved for the signal instance or termination is reached. For each iteration, one segment is processed at a time and typically in sequential order.

French Abstract

La presente invention concerne des techniques d'acquisition de la frequence d'une instance de signal basees sur une fenetre d'echantillons de donnees couvrant une periode de temps inferieure au temps necessaire

pour obtenir une frequence asservie. La fenetre d'echantillons de donnees est initialement capturee et stockee sur une memoire tampon d'echantillons. Un segment d'echantillons de donnees est ensuite extrait de la memoire tampon d'echantillons afin d'etre traite. Les echantillons de donnees extraits sont tournes d'une estimation d'erreur de frequence actuelle, afin de fournir des echantillons de donnees transposes en frequence qui sont traitees afin de produire un ou plusieurs symboles pilotes. Une estimation d'erreur de frequence mise a jour pour les echantillons de donnees transposes en frequence est ensuite derivee, sur la base des symboles pilotes, par utilisation d'une boucle de commande de frequence. La fenetre d'echantillons de donnees est traitee pour un certain nombre d'iterations, jusqu'a ce que l'acquisition de frequence soit effectuee pour l'instance de signal ou que ce soit la fin. Pour chaque iteration, un segment est traite a la fois et, generalement, dans un ordre sequentiel.

Legal Status (Type, Date, Text)

Publication 20030807 A1 With international search report.

Publication 20030807 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

Fulltext Availability:

Detailed Description

Detailed Description

... In this case, only "pertinent" data samples that may be used to derive a frequency **error** estimate are retrieved and processed, and remaining data samples may be omitted. These pertinent data **samples** are typically those for the **time period** when the gated pilot is transmitted (e.g., the data **samples** for the 96- **chip** pilot burst in each 1024- **chip** half-slot in IS-856). For a gated pilot transmission scheme, higher transmit power is...

...example, the accumulation interval may be selected to be 32, 16, 8, or even fewer **chips** for the gated pilot in IS [1085]

34/5,K/18 (Item 18 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00944030 **Image available**

SAMPLING METHOD FOR A SPREAD SPECTRUM COMMUNICATION SYSTEM
ECHANTILLONNAGE POUR UN SYSTEME DE COMMUNICATION A ETALEMENT DU SPECTRE

Patent Applicant/Assignee:

ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE (EPFL), SRI, CM Ecublens,
CH-1015 Lausanne, CH, CH (Residence), CH (Nationality), (For all
designated states except: US)

Patent Applicant/Inventor:

MARAVIC Irena, Av. du Mont d'Or 69, CH-1007 Lausanne, CH, CH (Residence),
YU (Nationality), (Designated only for: US)
VETTERLI Martin, Ch. de Baussan 11, CH-1603 Grandvaux, CH, CH (Residence)
, CH (Nationality), (Designated only for: US)
KUSUMA Julius, 748 Oakland Ave #400, Oakland, CA 94611, US, US
(Residence), ID (Nationality), (Designated only for: US)

Legal Representative:

SAAM Christophe (agent), Patents & Technology Surveys SA, Fbg du Lac 2,
P.O. Box 2848, CH-2001 Neuchatel, CH,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200278204 A1 20021003 (WO 0278204)

Application: WO 2002EP3390 20020326 (PCT/WO EP0203390)

Priority Application: EP 2001107530 20010326; EP 2001119537 20010815

Designated States: AE AG AL AM AT AT (utility model) AU AZ BA BB BG BR BY
BZ CA CH CN CO CR CU CZ CZ (utility model) DE DE (utility model) DK DK
(utility model) DM DZ EC EE EE (utility model) ES FI FI (utility model)
GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV
MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SK
(utility model) SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: H04B-001/707

International Patent Class: H03M-001/12

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 9090

English Abstract

Method for decoding a signal sent over a bandwidth-expanding communication system, where both channel estimation and signal detection are carried out on a set of samples generated by sampling the received signal at a sub-Nyquist rate, thus allowing for a significant reduction of the complexity of the sampling device of receivers using said method, as well as a significant reduction of their computational requirements.

French Abstract

La presente invention concerne un procede de decodage d'un signal envoye via un systeme de communication a expansion de la largeur de bande. En l'occurrence, pour calculer le canal et detecter le signal, on se fonde sur un jeu d'echantillons produits par echantillonnage du signal recu a une vitesse inferieure au Nyquist. Cela permet de reduire de facon considerable, d'une part la complexite de l'echantillonneur des recepteurs utilisant ce procede, et d'autre part la puissance de calcul

requisite.

Legal Status (Type, Date, Text)

Publication 20021003 A1 With international search report.

Publication 20021003 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

Fulltext Availability:

Claims

Claim

- ... detection, of a signal
sent over a bandwidth-expanding communication system from a set of **sampled** values generated by **sampling** the received wideband **signal** with a **sampling** frequency lower than the **sampling** frequency given by the Shannon's **sampling** theorem, but greater than the rate of innovation p of said sent signal, thus allowing a receiver using this method to **sample** the received **signal** at a sub-Nyquist rate and still allowing an exact reconstruction of the sent signal...
- ...or for signal detection are performed on the basis of a significantly reduced set of **sampled** values compared to the set of **sampled** values needed by current digital receivers, thus allowing a significant reduction of the computational requirements...
- ...fading and direction-of-arrival of the different signals, from a significantly reduced set of **sampled** values compared to the set of **sampled** values needed by current digital receivers.
The minimal **sampling** frequency required by the method according to the invention is determined by the rate of...
- ...equal to its symbol rate $1/T_b$, which, as explained before, is lower than its **chip** rate $1/T_c$ by the spreading factor. in the multi-user case, the rate of innovation...
- ...the rate of innovation p of the received signal is still significantly lower than its **chip** rate $1/T_c$.
The invention will be better understood with the help of the figures...
- ...convolved with a filtering signal $P(t)$, for instance a bandlimited sinc signal. The filtered **signal** 12 is then **sampled** at a regular **sampling** frequency $f_s = 1/T_s$, resulting in the time-continuous **sampled** **signal** $y_s(t)$. The **sampled** values $y[nT_s]$ are extracted from this time-continuous **sampled** **signal** $y_s(t)$ by a continuous-to-discrete converter d and the spectral values $Y[m]$ of the time-continuous signal $y_s(t)$ are computed from these **sampled** values $y[nT_s]$, for instance by using the Fast Fourier Transform (FFT) method. The spectral...a one-dimensional estimation problem including a set of spectral values

The

inventive method thus significantly reduces the required **sampling** frequency f , in comparison to current methods typically requiring digital receivers to **sample** the received **signal** at least at its **chip** rate VT ,

Consequently, the number of **sampled** values required by the inventive method for estimating the propagation parameters is also significantly reduced...

...to obtain a more precise estimation of the propagation parameters a_k (1) and r_k (1), the **sampling** frequency f , needs to be increased, while the length H of the training sequences b_{kt} remains the same. In the presence of noise, the **sampling** frequency f , required for good estimation accuracy depends on signal-to-noise ratio (SNR), yet in most cases encountered in practice that **sampling** frequency f , is still far below the **chip** rate $1/T$,
In a variant preferred embodiment, the method described above during the training phase...

...is not aligned to transmitted symbol b_k (h) boundaries.
Therefore, in the general case, the **sample** values $y[nT_s]$ from which the Fourier series coefficients $Y[m]$ are computed, will actually...

...as in the training phase 30, first filtered with a lowpass filter f and then **sampled** at a sub-Nyquist rate, that is, at a

sampling frequency f , lower than the **chip** rate $1/T_c$ of the received signal $y(t)$, but higher than its rate of innovation p . The inventive method base on the surprising finding that a set of **sampled** values generated from a signal $1/5$ at a sub-Nyquist rate is sufficient to reconstruct or to decode said signal, if said set of **sampled** values is generated at a **sampling** frequency f_s higher than the signal's rate of innovation p .

During the detection phase...

...over the transmission channel c . The second signal $y(t)$ is first filtered and then

sampled at a **sampling** frequency f , lower than the **sampling** frequency

given by the Shannon theorem, but higher than rate of innovation p of the ...

...equal

to the signal's information rate K/T_b , thus generating a second set of **sampled** values $y[nT_s]$. **Signal** detection is then performed with known detection methods such as for instance Minimum Mean Square Error (MMSE) or decorrelating detector, using the values of the second set **sampled** values $y[nT_s]$ and the previously estimated propagation parameters

(1) (1)

a_k and T_k

in...system proceeds to

the subsequent detection phase 40 without solving the series of one dimensional **estimation** problems for **estimating** each propagation parameter a_k (1) or T_0 . During the detection **phase** 40, the **second signal** $y(t)$

is **sampled** as described in the previous embodiment of the method, thus generating a second set of **sampled** values $y[nT_j]$ from which a second set

of spectral values $Y[m]$ can be...

- ...by the users k . The rate of innovation p of the signal $y(t)$ is then equal to its information rate K_{rrb} . The **sampling** frequency f_s must then be $f_s > p$.
- TS T_b which is still well below the **chip** rate $1/T_c$ of the received signal. In the case of noisy transmission, the propagation...
- ...In order to perform a better estimation of these channel parameters and therefore a less **bit error** rate, the **sampling** frequency f , should be higher than the rate of innovation p . The **sampling** frequency f , required for good estimation accuracy will then depend on signal-to-noise ratio (SNR), yet in most cases encountered in practice, that **sampling** frequency f_s is still far below the **chip** rate $1/T_c$. In a variant preferred embodiment of the method, the filtering signal 9...
- ...previously described embodiments of the method, first filtered with a lowpass filter f and then **sampled** at a frequency f , higher than the innovation rate p of the signal $y_i(t)$, but lower than the frequency given by Shannon's **sampling** theorem. As previously described, sets of spectral values $Y_i[m]$ are then computed from each generated set of **sampled values** y_i [nTs], for computing a matrix D_i with each said set of spectral values $Y_i[m]$, with the known values of the bits b_k (h...the known 2-D RAKE method but on a lowpass filtered version of the received **signals** $y_i(t)$ **sampled** at a **sampling** frequency f_s higher than the innovation rate p of the received signals $y_i(t)$, but lower than the frequency given by Shannon's **sampling** theorem. In a further preferred embodiment, the inventive method is applied to a CDMA communication...
- ...performed by first filtering the received signal $y(t)$ with a filter f and then **sampling** it at a frequency f_s lower than the frequency given by Shannon's **sampling** theorem, but higher than the rate of innovation p of the received 15 signal $y(t)$, for generating a set of **sampled** values y [nTs]. These **sampled** values y [nTs] are then processed by a bank of digital matched filters, each matched to the **sampled** lowpass filtered version of a user's coding sequence $S_k(t)$. As the lowpass filtered...

34/5,K/19 (Item 19 from file: 349)

DIALOG(R) File 349:PCT FULLTEXT

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00937410 **Image available**

METHOD AND APPARATUS FOR DIAGNOSING FAILURES IN AN INTEGRATED CIRCUIT USING DESIGN-FOR-DEBUG (DFD) TECHNIQUES

PROCEDE ET APPAREIL PERMETTANT DE DIAGNOSTIQUER DES PANNES DANS UN CIRCUIT INTEGRE A L'AIDE DE TECHNIQUES DE DEPANNAGE INTEGREES

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Patent and Priority Information (Country, Number, Date):
Patent: WO 200271567 A1 20020912 (WO 0271567)
Application: WO 2002US3413 20020228 (PCT/WO US0203413)
Priority Application: US 2001272064 20010301; US 200286214 20020227
Designated States: AU BR CA CN CZ ID IL IN JP KP KR MX NO NZ PL RO SG US VN
ZA
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: H02H-003/05

International Patent Class: H03K-019/003

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 19213

English Abstract

A method and apparatus for inserting design-for-debug (DFD) circuitries in an integrated circuit to debug or diagnose DFT modules, including scan cores, memory BIST (built-in self-test) cores, logic BIST cores, and functional cores. The invention further comprises using a DFD controller for executing a plurality of DFD commands to debug or diagnosis the DFT modules embedded with the DFD circuitries. When use alone or combined together, these DFD commands will detect or locate physical failures in the DFT modules in the integrated circuit on an evaluation board or system using a low-cost DFT debugger. A computer-aided design (CAD) method is further developed to synthesize the DFD controller and DFD circuitries according to the IEEE 1149.1 Boundary-scan Std. The DFD controller supports, but is not limited to, the following DFD commands: RUN SCAN, RUN MBIST, RUN LBIST, DBG SCAN, DBG MBIST, DBG LBIST, DBG FUNCTION, SELECT, SHIFT, SHIFT CHAIN, CAPTURE, RESET, BREAK, RUN, STEP,

and STOP.

French Abstract

L'invention concerne un procede et un appareil permettant d'introduire des circuits de conception de depannage (DFD) dans un circuit integre afin de depanner et de diagnostiquer des modules de conception d'essai (DFT) comprenant des noyaux de balayage, des noyaux BIST (essai automatique integre) de memoire, des noyaux BIST logiques, et des noyaux fonctionnels. L'invention concerne egalement une unite de commande DFD permettant d'executer une pluralite de commandes DFD afin de mettre au point ou de diagnostiquer les modules DFT incorpores dans les circuits. Lorsqu'on les utilise seules ou associees, les commandes DFD detectent ou localisent des defaillances physiques dans les modules DFT du circuit integre sur un systeme ou un tableau d'evaluation a l'aide d'un depanneur DFT bon marche. L'unite de commande DFD supporte, notamment, les commandes suivantes: RUN<u> </u>SCAN, RUN<u> </u>MBIST, RUN<u> </u>LBIST, DBG<u> </u>SCAN, DBG<u> </u>MGIST, DBG<u> </u>LBIST, DBG<u> </u>FUNCTION, SELECT, SHIFT, SHIFT<u> </u>CHAIN, CAPTURE, RESET, BREAK, RUN, STEP, et STOP.

Legal Status (Type, Date, Text)

Publication 20020912 A1 With international search report.

Examination 20030306 Request for preliminary examination prior to end of 19th month from priority date

Fulltext Availability:

Claims

Claim

- ... a MBIST (memory BIST) clock, with
an embedded DFD (design-for-debug) circuitry in an
integrated circuit ; said method comprising the steps of:
(a) issuing a DBG -MBIST command for generating a...
- ...circuitry in said memory BIST cores;
(c) issuing a SKIP command for signaling the memory
BIST controller in selected said memory **BIST** core to skip
a predetermined number of MBIST **clock cycles** or errors;
(d) issuing a RUN command for generating a run
control signal to continue the memory **BIST** operation of
said memory **BIST** controller in each said memory **BIST** core
whenever a new **error** is **found** and said predetermined number
of MBIST **clock cycles** or errors are reached;
(e) issuing a CAPTURE command for capturing selected
data in said memory **BIST** cores into a plurality of MBIST
debug registers in said DFD circuitries over a
predetermined **sampling** period;
(f) issuing a SHIFT command for shifting out said
selected data in said MBIST...
- ...SHIFT command for selectively
shifting in expected responses of said seed registers for
on- **chip** comparison or shifting out output responses of said
seed registers for off- **chip** comparison over a predetermined
sampling period;
(f) issuing a third SHIFT command for shifting in
selected new seeds, each comprising a new predetermined
number of LBIST **clock cycles** , to said seed registers;
(g) repeating steps of (d)-(f) until logic **BIST**
diagnosis is done; and

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DIALOG(R)File 349:PCT FULLTEXT
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00764517 **Image available**

FADE MARGIN TEST

ESSAI DE MARGE CONTRE LES EVANOUISSEMENTS

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Stockholm, SE

Patent and Priority Information (Country, Number, Date):

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Application: WO 2000SE1215 20000609 (PCT/WO SE0001215)

Priority Application: SE 992209 19990611

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DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC

LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI

SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: H04B-017/02

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 5196

English Abstract

According to the invention, a fade margin test value for a radio link is calculated according to a routine whereby the output power of the transmitter is gradually decreased until the forward error correction activity FCA reaches a predetermined value, FCA1, whereupon the output power is regulated back to a duty level again. The reduction in output power is performed when the link is operating in a normal way, i.e. while communication may be transmitted on the link. Subsequently, a fade margin test value FM is determined as the ratio related to the nominal output power and the output power corresponding to the predetermined forward error correction value FCA1 at the reduced power level. Finally, the output power is increased to nominal output power.

French Abstract

Selon l'invention, on calcule pour une liaison radio la valeur d'un essai de marge contre les evanouissements, a l'aide d'un programme permettant de diminuer graduellement la puissance de sortie de l'emetteur jusqu'a ce que l'activite de correction d'erreur sur voie directe FCA atteigne une valeur determinee FCA1, auquel cas la puissance de sortie est reglee pour revenir a une puissance de niveau de travail. La reduction de la puissance de sortie s'effectue lorsque la liaison fonctionne de maniere normale, c'est-a-dire pendant qu'une communication peut etre transmise sur la liaison. Ulterieurement, une valeur d'essai FM de marge contre les evanouissements est determinee en tant que rapport entre la puissance de sortie nominale et la puissance de sortie correspondant a la valeur de

correction d'erreur sur voie directe FCA1 a un niveau de puissance reduite. Enfin, la puissance de sortie est augmentee pour atteindre la puissance de sortie nominale.

Legal Status (Type, Date, Text)

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Publication 20001221 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.

Examination 20010315 Request for preliminary examination prior to end of 19th month from priority date

Fulltext Availability:

Claims

Claim

... a first embodiment according to the invention, Fig. 3 is a schematic representation of the **bit error** rate, respectively before and after performance of forward error correction, as a function of input...

...be described with reference to fig. 3. In the example shown on fig. 3, the **bit error** rate of the input signal has been shown as a function of the input power...

...forward error correction has been performed in the receiver. The graph designated A1 represents the **bit error** rate before forward error correction, while the graph A2 represents the **bit error** rate after forward error correction. For illustrative purposes, the graphs have been drawn as straight...

...that the input power at the receiver is decreased. Hence, the expected variations in the **bit error** rate can be found from assessing the variation in the input power level, corresponding to the weather caused attenuation and reading the **bit error** rate which appears from graph A2.

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Graphs A1 and A2 may for instance correspond...

...the given noise level. In fact, the fade margin is chosen so high that a **bit error** rate above BER (Aw) (the **bit error** rate corresponding to the assessed worst case level, Rfinw) is sufficient unlikely to occur. Now...

...right. The new situation is represented, by way of example by graph 131, representing the **bit error** rate before forward error correction and graph B2, after forward error correction. It is noted that under the new enhanced noise level the worst case **bit error** rate It should be noted that the graphs and corresponding **bit error** rates shown in fig. 3 are only exemplary and that they do not necessarily represent...

...schematic. As mentioned above, the network provider typically seeks a guarantee for a desired maximum **bit error** rate after forward error correction.

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As appears from graphs A1 I A29 B1 and B2, a certain given forward error correction activity, FCA, corresponds to a certain **bit error** rate, BER . If for instance the maximum acceptable **bit error** rate is BER (1) (10×10^{-5}), the corresponding forward error correction activity is found as the vertical...

...case situation occurs, under the noise level given by B, it is seen that the **bit error** rate after correction would amount to the "unacceptable" level **BER** (Bw) ($10\exp-4$) if the attenuation accounted for as low a value as Rfinw. It...

...The above routine would advantageously have a relatively short duration. Hence, the cumulative number of **bit errors** will only increase insignificantly due to the extra errors, which are "produced" during the routine...

...value FCA1 which corresponds to an input power Rf_{in1} (B), for which the corresponding **bit error** rate per definition amounts for **BER** (1), ($10\exp-5$), which is still within ample distance from the lower critical value of...

...the calculated fade margin test value $FM(t)$ approaches or falls below W, the effective **bit error** rate would assert the critical value of the maximum desired **BER** value. In fig. 4, is a schematic representation of the input power level according to...

...certain value for a certain period. Thereby it is accomplished that the cumulative number of **bit errors** generated under the first routine can be kept very low. The first routine is only **BER** are monitored. Should any of these values reach critical level the fade margin routine is...

...points in time denoted by arrows S. Alternatively, a statistical method may be used for **finding** the applicable fade **error margin test** values, i.e. whereby the minimum values P_{out1} within a predetermined **time interval** are identified. It would be clear to the person skilled in the art that signals...

34/5,K/30 (Item 30 from file: 349)
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00510363 **Image available**

PORTABLE OBJECT SUCH AS A CARD WITH MICROCIRCUIT COMPRISING MEANS FOR
MONITORING COMMANDS APPLIED THERETO

OBJET PORTATIF DE TYPE CARTE A MICROCIRCUIT COMPRENANT DES MOYENS DE
SUPERVISION DES COMMANDES QUI LUI SONT APPLIQUEES

Patent Applicant/Assignee:

INNOVATRON,
MORENO Roland,

Inventor(s):

MORENO Roland,

Patent and Priority Information (Country, Number, Date):

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SE

Main International Patent Class: G07F-007/10

Publication Language: French

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 2088

English Abstract

The invention concerns a portable object (10) comprising an interface receiving signals (VCC; CLK; RST) representing commands applied to the **microcircuit** (10) and signal (I/O) representing data to be processed by said **microcircuit**. Means (16, 26, 22) monitor for a given **time interval** the external application of at least one of said commands, said means being capable of **detecting** an **abnormally** repeated application of said command relative to a predetermined criterion and of selectively inhibiting, on the basis of said detection, the processing of the received data by the **microcircuit**. The monitored command can be the reset (RST) signal and/or the clock signal (CLK), and the given time interval, the interval between consecutive switching on and switching out of the portable object, the monitoring means (16, 26) operating by counting successive applications of the command, the predetermined criterion being the overshooting of the count value.

French Abstract

Cet objet portatif (10) comporte une interface recevant des signaux (VCC, CLK, RST) representatifs de commandes appliquees au microcircuit (10) et des signaux (I/O) representatifs d'informations a traiter par ce microcircuit. Des moyens (16, 26, 22) supervisent pendant une periode de temps donnee l'application depuis l'exterieur d'au moins l'une des commandes, ces moyens etant aptes a detecter une application anormalement repetee de cette commande par rapport a un critere predefini et a inhiber selectivement, en fonction de cette detection, le traitement par le microcircuit des informations recues. La commande supervisee peut etre le signal de remise a zero (RST) et/ou le signal d'horloge (CLK), et ladite periode de temps donnee, la periode de temps comprise entre une mise sous tension et une mise hors tension consecutive de l'objet portatif, les moyens de supervision (16, 26) procedant par comptage des applications successives de la commande, ledit critere predefini etant le depassement

d'une valeur de compte donnee.

English Abstract

...object (10) comprising an interface receiving signals (VCC; CLK; RST) representing commands applied to the **microcircuit** (10) and signal (I/O) representing data to be processed by said **microcircuit** . Means (16, 26, 22) monitor for a given **time interval** the external application of at least one of said commands, said means being capable of **detecting** an **abnormally** repeated application of said command relative to a predetermined criterion and of selectively inhibiting, on the basis of said detection, the processing of the received data by the **microcircuit** . The monitored command can be the reset (RST) signal and/or the clock signal (CLK...

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DIALOG(R)File 349:PCT FULLTEXT
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00444981 **Image available**

METHOD AND APPARATUS FOR GENERATING AN INTERNAL CLOCK SIGNAL THAT IS
SYNCHRONIZED TO AN EXTERNAL CLOCK SIGNAL
PROCEDE ET DISPOSITIF POUR GENERER UN SIGNAL D'HORLOGE INTERNE SYNCHRONISE
AVEC UN SIGNAL D'HORLOGE EXTERNE

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Inventor(s):

MANNING Troy A,

Patent and Priority Information (Country, Number, Date):

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Application: WO 98US2233 19980211 (PCT/WO US9802233)

Priority Application: US 97798226 19970211

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GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG
MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN
YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH DE
DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE
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International Patent Class: G06F-01:10; H03K-05:135

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 5234

English Abstract

A clock generator circuit for an **integrated circuit** constituting a phase-locked-loop (PLL) includes a phase detector comparing the phase of a delayed external clock signal to the phase of an internal clock signal. An error signal corresponding to the difference in phase between the two clock signals is applied to a differential amplifier where the error signal is offset by a value corresponding to the delay of an external clock signal as it is coupled to the phase **detector**. The offset **error** signal is applied to a control input of a voltage controlled oscillator which generates the internal **clock** signal. The **phase** of the internal **clock** signal is thus adjusted so that it is substantially the same as the phase of the external clock signal before being delayed as it is coupled to the phase detector and other circuitry in the **integrated circuit**. The voltage controlled oscillator is constructed to operate in a plurality of discrete frequency bands so that the offset error signal need only control the frequency of the internal clock signal over a relatively small range. The frequency band is selected by a signal from a register that is programmed by a user with data identifying the frequency of the external clock signal.

French Abstract

Un circuit generateur d'horloge, destine a un circuit integre constituant un circuit a phase asservie (PLL), comprend un detecteur de phase qui compare la phase d'un signal d'horloge decale a la phase d'un signal d'horloge interne. Un signal d'erreur correspondant a la difference de phase entre les deux signaux d'horloge est applique a un amplificateur differentiel, au niveau duquel il est decale d'une valeur correspondant a la temporisation d'un signal d'horloge externe au moment ou celui-ci est couple au detecteur de phase. Le signal d'erreur decale est applique a l'entree de commande d'un oscillateur commande en tension, qui genere le signal d'horloge interne. La phase du signal d'horloge interne est ainsi ajustee, de facon a etre sensiblement la meme que celle du signal d'horloge externe avant que celui-ci soit decale au moment ou il est couple au detecteur de phase et a d'autres circuits du circuit integre. L'oscillateur commande en tension est configure de facon a fonctionner dans une pluralite de bandes de frequence discrete, si bien que le signal d'erreur decale ne commande la frequence du signal d'horloge interne que sur une plage relativement etroite. La bande de frequence est selectionnee par un signal provenant d'un registre que l'utilisateur programme au moyen des donnees identifiant la frequence du signal d'horloge externe.

English Abstract

A clock generator circuit for an **integrated circuit** constituting a phase-locked-loop (PLL) includes a phase detector comparing the phase of a...

...to the delay of an external clock signal as it is coupled to the phase **detector**. The offset **error** signal is applied to a control input of a voltage controlled oscillator which generates the internal **clock** signal. The **phase** of the internal **clock** signal is thus adjusted so that it is substantially the same as the phase of...

...being delayed as it is coupled to the phase detector and other circuitry in the **integrated circuit**. The voltage controlled oscillator is constructed to operate in a plurality of discrete frequency bands...

34/5,K/34 (Item 34 from file: 349)

DIALOG(R) File 349:PCT FULLTEXT

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00430246 **Image available**

RESETTABLE SAFETY CIRCUIT FOR PTC ELECTRIC BLANKETS AND THE LIKE
CIRCUIT DE SECURITE A REENCLENCHMENT POUR COUVERTURE ELECTRIQUE A
COEFFICIENT POSITIF DE TEMPERATURE ET ANALOGUE

Patent Applicant/Assignee:

MICRO WEISS ELECTRONICS,

Inventor(s):

WEISS John,

Patent and Priority Information (Country, Number, Date):

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Application: WO 97US20134 19971106 (PCT/WO US9720134)

Priority Application: US 96745884 19961108

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Publication Language: English

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Detailed Description

Claims

Fulltext Word Count: 11643

English Abstract

A safety-assuring control device for an electric blanket which includes a PTC heater includes an **integrated circuit** microcontroller unit having first and second safety circuit inputs and an output connected to a control input of an electrically controlled heater switch. A neon tube (N101) is connected between the primary safety link return conductor of the heater and the first safety circuit input (122) to indicate whether there is a first type of fault in the PTC heater. A connection between the second safety circuit input (123) and the secondary safety link return conductor of the PTC heater is provided which indicates whether there is a second type of fault in the heater. The microcontroller unit (IC114) includes a preliminary **fault detection** circuit for supplying a limited power test signal in a test mode to the heater for predetermined **period of time** prior to a full power operation of the heater. The microcontroller unit (IC114) also includes a circuit for controlling operation of the microcontroller unit to terminate supply of current to the heater if at least one **fault is detected** by the microcontroller at least one of the first and second safety circuit inputs (122, 123) during the predetermined **period of time**, and for controlling operation of the microcontroller unit to supply current to the heater in the full power operation if no **fault is detected** during the predetermined **period of time**.

French Abstract

Ce dispositif de commande de securite destine a une couverture electrique comporte un generateur de chaleur a coefficient positif de temperature (PTC) comprenant un microcontroleur a circuit integre possedant une premiere et une seconde entree de circuit de securite et une sortie connectee a une entree de commande d'un commutateur de generateur de chaleur commande electriquement. Un tube au neon (N101) est connecte aux bornes d'un conducteur primaire de retour de liaison de securite du generateur de chaleur et de la premiere entree du circuit de securite (122) afin d'indiquer s'il est survenu un premier type de defaillance dans le generateur de chaleur PTC. Une connexion reliant la seconde entree du circuit de securite (123) et le conducteur secondaire de retour de liaison de securite du generateur de chaleur PTC permet d'indiquer s'il est survenu un second type de defaillance dans le generateur de chaleur. Le microcontroleur (IC114) comporte un circuit de pre-detection de defaillance destine a fournir un signal d'essai a alimentation limitee dans un mode essai au generateur de chaleur pendant un laps de temps predetermine avant le fonctionnement du generateur de chaleur a pleine puissance. Le microcontroleur (IC114) comporte egalement un circuit destine a agir sur son fonctionnement afin de faire cesser l'alimentation en courant du generateur de chaleur si une defaillance est detectee dans la premiere ou la seconde entree (122, 123) du circuit de securite durant le laps de temps predetermine, ainsi qu'a agir sur son fonctionnement afin de fournir du courant au generateur de chaleur fonctionnant a pleine puissance si aucune defaillance n'a ete detectee durant le laps de temps predetermine.

English Abstract

...safety-assuring control device for an electric blanket which includes a PTC heater includes an **integrated circuit** microcontroller unit having first and second safety circuit inputs and an output connected to a...

...a second type of fault in the heater. The microcontroller unit (IC114) includes a preliminary **fault detection** circuit for supplying a limited power test signal in a test mode to the heater for predetermined **period of time** prior to a full power operation of the heater. The

microcontroller unit (IC114) also includes...

...the microcontroller unit to terminate supply of current to the heater if at least one **fault** is **detected** by the microcontroller at least one of the first and second safety circuit inputs (122, 123) during the predetermined **period** of **time**, and for controlling operation of the microcontroller unit to supply current to the heater in the full power operation if no **fault** is **detected** during the predetermined **period** of **time**.

34/5,K/35 (Item 35 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00406184 **Image available**

3-BRAIN ARCHITECTURE FOR AN INTELLIGENT DECISION AND CONTROL SYSTEM

ARCHITECTURE A TROIS CERVEAUX POUR SYSTEME INTELLIGENT DE COMMANDE ET DE DECISION

Patent Applicant/Assignee:

WERBOS Paul J,

Inventor(s):

WERBOS Paul J,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9746929 A2 19971211

Application: WO 97US9724 19970604 (PCT/WO US9709724)

Priority Application: US 9619154 19960604

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES

FI GB GE HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW

MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG US UZ VN GH KE LS

MW SD SZ UG AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE

IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG

Main International Patent Class: G06F-015/18

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 84125

English Abstract

A method and system (100) for intelligent control of external devices using a mammalian brain-like structure having three parts. The method and system include a computer storage medium (19) for storing a computer program code which causes the computer (102) to implement a neural network system which is an extension of the model-based adaptive critic design and is applicable to real-time control (e.g., robotic control) and real-time distributed control. Additional uses include data visualization, data mining, and other tasks requiring complex analysis of inter-relationships between data.

French Abstract

L'invention concerne un procede et un systeme de commande intelligente pour dispositifs externes, faisant appel a une structure en trois parties, analogue a la configuration cerebrale des mammiferes, comprenant un reseau neuronal informatique qui est un developpement de la conception critique adaptative a base de modeles et qui est utilisable pour la commande en temps reel (par exemple la commande de robots) et la commande repartie en temps reel. D'autres utilisations sont possibles, a savoir: visualisation ou extraction des donnees, et autres taches necessitant une analyse complexe des relations mutuelles entre les donnees.

Fulltext Availability:
Claims

Claim

... t_{4-1} to time t , as implicitly assumed in equation 12. But in a real- **time** control system, the **interval** between **time** t and time $t+1$ (the **sampling** interval) may be very short. The literature on artificial intelligence has stressed the need to...Thus after n complete value updates, the "critic" (the estimate of J) "sees" only n **periods** of **time** into the future, in effect. Equation 13 is just an **estimate** of the true value:
 $J(I - Mr,) - 1 U(14)$
In order to learn the...are exact; by contrast, equation 32 involves the usual random disturbances associated with any statistical **sampling** method, without any real cost advantage.
1,4 From Passive Desi@jn to Active Desi...the adaptation methods in the adaptive critic literature, one can use -- in theory -- "almost any" **sampling** strategy which is mixed and diverse enough to eventually touch base with all relevant states...important in some cases. Thirdly, the operations described above -- including the use of forwards results **sampling** in order to evaluate possible decisions and to train decision networks -- clearly require the existence... v_0 and a vector $-v$, representing:
 $J - ZVO + E V r$
 $I_{ii}(51)$
The **LSI** approach is not a viable alternative to QSI, because it cannot represent the wide variety...
...needed for a flexible planning system. However, it is very plausible to consider adding an **LSI** object to the QSI objects, to provide additional guidance to a decision block based on...brain: an engineering interpretation. For reasons discussed therein, this system cannot operate at the maximal **sampling** rate which the underlying hardware seems capable of. In order to perform true maximal-rate...so on. Neural network implementations of ADP also permit the use of high-throughput ANN **chips**, which can make it more practical to use a highly complex and intelligent control design...that the best existing ZIP code recognizers are based on ANNs, which, because of special **chips**, can also overcome the high throughput bottleneck, without requiring costly hard-wired application-specific **chips**. (See L.D.Jackei et al, Hardware requirements for neural-net optical character recognition, IJCNN90 Proceedings, IEEE, 1990, p.II II) (The adjustable weights in ANN **chips** make them usable on multiple applications, and even permit remote "reprogramming" based on telemetry.) Remote...time control under noise, minimizing fuel use (and pollution), is a central issue; likewise, special **chips** are called for. (In testimony in the summer of 1993 to Marilyn Lloyd's committee...appropriate for this particular task.
In practical applications today, computations are mainly based on discrete **time cycles** or **sampling** rates, rather than differential equations. In the discrete time formulation, t_{ki} are two related...between " t " and " $t+1$ " is 1/32 second. We might use a fast neural **chip**, allowing a thousand iterations of recurrent processing per frame, such

that the time between "n...

...style of

computation, with a high-speed inner recurrent loop embedded within a lower-speed **sampling** system, in order to perform the same task. For the maze problem, however, we were...has shown how cellular networks in general have far better throughput than conventional networks in **VLSI** implementation. Our design here does not seem very brain-like, but can we be sure...applications of such networks, it is important to consider the clock rates of computation and **data sampling**. For that reason, it is both easier and better to use error minimizing designs based...n represents a faster kind of time, like the computing cycle of a fast electronic **chip**. For example, if we build a computer to analyze images coming from a movie camera...

...per second coming

into the neocortex.) But if we use a fast neural network **chip**, the computational cycle --- the time between "n" and "n + 1" --- could be as small as...the derivative calculations, no matter how the derivatives are calculated. But in engineering, using fast **chips**, it does have some advantages -- not least of them, exactness. Still, it cannot address noise...

...efficient

manner, and the cost of the computations can become a problem, especially when millisecond **sampling** times are required. The adaptive critic approach -- broadly defined -- is the only type of design...should be reduced, and brain like approaches should become more and more attractive. New neural **chips** will also play a role. At the coarsest level, the "ladder" consists of three types...lower-level adaptive critic system. However, because the lower system is based on a higher **sampling** rate, one would expect it to add in a few additional components of utility, such...training signals to the cerebellum from the olive do seem to involve a low-frequency **sampling** rate (like that of the upper brain), even though the cerebellum itself operates with an...

34/5,K/36 (Item 36 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00355275 **Image available**

**MITIGATION OF MULTIPATH EFFECTS IN GLOBAL POSITIONING SYSTEM RECEIVERS
ATTENUATION DES EFFETS DES TRAJECTS MULTIPLES DANS LES RECEPTEURS DE
SYSTEMES GPS**

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HATCH Ronald Ray,
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Inventor(s):

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Patent and Priority Information (Country, Number, Date):

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Application: WO 96US7774 19960524 (PCT/WO US9607774)
Priority Application: US 95449215 19950524

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NL PT SE

Main International Patent Class: G01S-001/04

International Patent Class: H04B-01:707

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 29660

English Abstract

A technique for minimizing or eliminating the effect of multipath signals in a receiver processing pseudorandom (PRN) code signals, such as in a global positioning system (GPS) receiver. The presence of multipath signals adversely affects both code measurements and carrier phase measurements of received PRN signals. One aspect of the invention provides for improved code tracking in the presence of multipath signals, by sampling the received code with a multipath mitigation window (MMW) (FIG. 25D) that results in a code error function (FIG. 25F) that reduces or eliminates the multipath effects. The MMW, which may be any of a number of preferred waveforms (FIGS. 35b-35E), provides a code error function that varies in opposite directions from zero at a desired tracking point (402), but assumes a nearly zero value when the MMW is advanced from the tracking or synchronization point by more than a small fraction of a code chip. Because of this nearly zero code error value on the early side of the desired tracking point, delayed multipath signals will have a corresponding code error function that is nearly zero (FIG. 25F) at the desired tracking point of the directly received signals, and the multipath signals will, therefore, have little or no effect on the desired tracking point and on code synchronization. The effects of multipath signals on carrier phase measurements are minimized by sampling the received signals, together with their possible multipath components, before and immediately after code transitions (vectors A and B, respectively). The vector relationship of the directly received (D) and multipath (M) signals is such that performing a vector average of the two types of samples (A and B) produces the directly received signal (D) and its correct phase, with many, if not all, of the multipath components (M) eliminated.

French Abstract

L'invention a pour objet une technique pour minimiser ou supprimer l'effet des signaux a trajets multiples dans des signaux de code de bruit pseudo-aleatoire lors du traitement par le recepteur, tel qu'un recepteur d'un systeme GPS. La presence de signaux a trajets multiples affecte negativement les mesures des codes et les mesures de phases porteuses des signaux de code de bruit pseudo-aleatoire. Selon un aspect de l'invention, il est possible d'ameliorer la poursuite du code en presence de signaux a trajets multiples, en echantillonnant le code recu par une fenetre d'attenuation des effets des trajets multiples (figure 25D), ce qui permet d'obtenir une fonction d'erreur de code (figure 25F) qui reduit ou supprime les effets des trajets multiples. La fenetre d'attenuation des effets des trajets multiples, qui peut presenter

n'importe laquelle parmi un nombre de formes d'ondes preferees (figures 35B-35E), fournit une fonction d'erreur de code qui varie dans des sens opposes a partir de zero au niveau d'un point de poursuite requis (402) mais adopte une valeur proche de zero lorsque l'on fait avancer la fenetre depuis le point de poursuite ou de synchronisation selon plus d'une petite fraction d'une puce de code. Du fait de cette valeur d'erreur de code proche de zero au debut du point de poursuite requis, des signaux a trajets multiples temporises vont presenter une fonction d'erreur de code correspondante qui est proche de zero (figure 25F) au niveau du point de poursuite requis des signaux directement recus, et les signaux a trajets multiples vont, par consequent, avoir peu ou pas d'effet sur le point de poursuite requis et sur la synchronisation du code. Les effets des signaux a trajets multiples sur les mesures des phases porteuses sont minimises par echantillonnage des signaux recus, avec leurs eventuelles composantes de trajets multiples, avant et immediatement apres les transitions de codes (vecteurs A et B, respectivement). La relation vectorielle des signaux a trajets multiples (M) et des signaux (D) directement recus est telle que la realisation d'une moyenne vectorielle de deux types d'echantillons (A et B) produit le signal directement recu (D) et sa phase correcte, tandis qu'un grand nombre, voire meme la totalite, des composantes (M) des trajets multiples sont supprimees.

Fulltext Availability:
Detailed Description

Detailed Description

... within a C/A code chip and 4 within a P code chip. With this clock , the phase MMW samplers of FIGS. 30B and 30D could be as narrow as 0.025 (1/40) of a C/A code chip . Therefore, the signal energy processed during either interval A or interval B is 0.025 times the energy processed during an entire C/A code chip , which results in a signal-to-noise (S/N) power reduction of 16 dB.

Fortunately...

34/5,K/37 (Item 37 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00234265 **Image available**

SYSTEM FOR DIVIDING PROCESSING TASKS INTO SIGNAL PROCESSOR AND
DECISION-MAKING MICROPROCESSOR INTERFACING
SYSTEME DE SEPARATION DES TACHES DE TRAITEMENT EN TACHES POUR INTERFACAGE
AVEC UN PROCESSEUR DE SIGNAUX ET UN MICROPROCESSEUR DE PRISE DE
DECISION

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Inventor(s):
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Patent and Priority Information (Country, Number, Date):

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Priority Application: US 91776161 19911015

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International Patent Class: G06F-09:40

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 219172

English Abstract

Architectures and methods are provided for efficiently dividing a processing task into tasks for a programmable real time signal processor (SPROC) (10) and tasks for a decision-making microprocessor (2120). The SPROC is provided with a non-interrupt structure where data flow is through a multiported central memory. The SPROC is also programmed in an environment which requires nothing more than graphic entry of a block diagram of the user's design. In automatically implementing the block diagram into silicon, the SPROC programming/development environment accounts for and provides software connection and interfaces with a host microprocessor (2120). The programming environment preferably includes: a high-level computer screen entry system which permits choosing, entry, parameterization, and connection of a plurality of functional blocks; a functional block cell library (2015) which provides source code representing the functional blocks; and a signal processor scheduler/compiler (2040) which uses the functional block cell library (2015) and the information entered into the high-level entry system to compile a program and to output source program code for a program memory and source data code for the data memory of the SPROC, as well as a symbol table which provides a memory map which maps SPROC addresses to variable names which the microprocessor (2120) will refer to in separately compiling its program.

French Abstract

On decrit des architectures et procedes qui permettent de separer efficacement une tache de traitement en taches destinees a un processeur de signaux programmable fonctionnant en temps reel (SPROC) (10) et a un microprocesseur de prise de decision (2120). Le SPROC est dote d'une structure depourvue d'interruption ou le flux de donnees arrive par l'intermediaire d'une memoire centrale a ports multiples. Il est aussi programme dans un environnement n'exigeant rien d'autre que l'introduction graphique d'un schema global relatif aux intentions de l'utilisateur. Avec la realisation automatique du schema global dans le silicium, l'environnement de programmation et de developpement du SPROC prend en compte et fournit la connexion au logiciel et realise une interface avec un microprocesseur hote (2120). Cet environnement de programmation comporte de preference un systeme d'introduction a ecran d'affichage perfectionne qui permet de choisir, introduire, parametriser et fournit une connexion avec differents blocs fonctionnels; une bibliotheque a cellules de bloc fonctionnel (2015) qui fournit un code source representant les blocs fonctionnels; et un programmeur/compilateur pour processeur de signal (2040). Ce dernier utilise la bibliotheque a cellules (2015) et l'information introduite dans le systeme d'introduction perfectionne pour compiler un programme et delivrer en sortie un code de programme source concernant une memoire du programme et un code de donnees source destine a la memoire de donnees du SPROC, ainsi qu'une table de symboles qui fournit une cartographie memorisee, contenant les adresses donnees par le SPROC aux differents noms auxquels le microprocesseur (2120) viendra se referer en compilant separement son propre programme.

Fulltext Availability:

Claims

Claim

... The program RAM bus 155 is comprised of a data bus of width twenty-four **bits** , and an address bus of ten bit width where a 1K program RAM is utilized...and DFreg 464 are. coupled to a flag bus 198 which is written to each **time** predetermined locations in the data RAM 125 are addressed as hereinbefore. described with reference to...The data (D) input into the D type flip-flop 667 should be the msb (**bit** twenty-three) of the data word being input into the DFMs data RAM buffer by...serial input port 700a. upon configuration during boot-up of the SPROC 10. The seven **bits** are defined as follows-.

dwl dw0

dw0 0 0 24 bits data width

I dwl...bit words and processes them in a manner described below with reference to a sixteen **bit** processor. Where the host processor is a twentyfour bit processor as indicated by mode pins...

...the data input register 812 in order to provide the SPROC with a twenty-four **bit** signal. Regardless of how the data input register ... the opposite function of multiplexer 8 1 0. When sending data to the twenty-four **bit** host processor, the demultiplexer 840 simply takes its twenty-four **bits** and passes them unchanged. When sending data to a sixteen bit host processor, the SPROC...

...sending data to an eight bit host processor, the SPROC 10 divides its twenty-four **bit** word into three eight bit bytes. In the master mode, on the "host" side of...

...of the EPROM can be accessed. When the EPROM places its data onto the data **locations** of the host bus 165, that data is forwarded through data multiplexer 8 10, and...with a 16-bit (64K) address bus. The port allows for 8-,16-, or 24- **bit** parallel data transfers between the SPROC chip and an external controller, memory-mapped peripheral, or...flags set in the parallel port status register. The parallel port input register, a 24- **bit** register, holds the data word received during a read operation for subsequent storage at the...this duration can be stretched to 5 master clock cycles for slower peripherals by setting **bit** 6 of the mode, register (the RX strobe. delay bit). Similarly, when the master SPROC...hardware and software tools for use with a PC to create, test, and debug digital **signal** processing designs. It was created as a design tool to support the development of code...CMULT?

CMULT

3 1

4 2

WINK

Function: The dsink cell accumulates two series of **input samples** (each size determined by the length parameter) into two blocks of data RAM. The blocks...

...data RAM locations

Icon:

SINK?

DSINK

DSINKRD

Function: Tha dsinkrd cell accumulates two series of **input samples** (each size determined by the length parameter) into two blocks of data RAM. The blocks...

...5, the cell is held in reset, otherwise the cell can capture a series: of **input samples** . The done output is zero if the cell is reset or capturing **input samples** , else the done output is one. The done output

needs to be terminated, either by...input < 2.0 (fixedpointformat)

Parameters:

Required: none

Optional: none

OrCAD Macro Keys: None, defined

Execution **Time** :

In line: code **duration** is 47 cycles maximum

Subroutine: code duration is 50 cycles maximum.

Resource Usage

In line: 52programRAMLocations

8 data RAM **locations**

Subroutine: (4 4LoiUmstances) + 50 program RAM locations

(4 of instances) + 5 data RAM locations

Icon:

LN?

2 n I

LN

SINK

Function: The sink cell accumulates a series of **input samples** (size determined by the length parameter) into a block of data RAM. The block is...

...data RAM locations.

icon:

SINK?

SINK

SINJKRD

Function: The sinkrd cell accumulates a series of **input samples** (size determined by the length parameter) into a block of data RAM. The block is...

...0.5, the cell is in reset otherwise the cell can capture a series of **input samples**. The done output is zero if the cell is reset or capturing **input samples**, else the done output is one. Reset is only effective when the sink block is...

...directory, before scheduling. Source reads the samples one at a time from the block in **data** RAM, and the number of **samples** is specified by the length parameter. The block's position in RAM begins at symbolic...

...instance-name.invector'. This block (vector) is accessible from an external microprocessor. Values of the **sample data** must be in the range from 0 to < 2.0 fixed point, but values can file of **data samples**, e.g. "filblock.dat"

trigger= SIPTORT I SIPTORTI I c10 I c1 1 1 c121 c13

rate = **sample** rate of trigger in Hz

Optional: length = 1 <= length <= 512 (default: length = 128)

zone alphanumeric...

...provides software components necessary to develop microprocessor applications in ANSI C that include the SPROC **chip** as a memorymapped device. Using the development system the designer captures the signal processing subsystem...slice or number of time slices. Operations that require longer than the length of one **time** slice must be completed over multiple **time** slices allotted to that operation. In the same way that time slices are allotted to...adding one more instance would require the GSP to take more than its allowed processing **time**; i.e. one **sample** period. Succeeding child instances are assigned to a new GSP, and the process continues until...design into data structures
top-group = iwgroup(design
name);

```

if (top-group == NULL) (
fprintf(stderr, " Error  loading U. WI, design
name);
fclose(outfp);
exit(EXFAILURE);
printf (l1kn11);
/* free temporary memory used...BOOLEAN symroo2interface( unsigned char @
symbol.rec)
BOOLEAN ret.val;
1* special case of spaces for - zone field means can't probe signal
if (symbol-ree[INTERFACE.SYM-COL]
ret.val a TRUE;
else
ret val = FALSE...
? t34/5,k/40

```

34/5,K/40 (Item 40 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00131124

ERROR DETECTION AND CORRECTION SYSTEM

SYSTEME DE DETECTION ET DE CORRECTION D'ERREURS

Patent Applicant/Assignee:

NCR CORPORATION,

Inventor(s):

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SCHMIDT Carson Thomas,

Patent and Priority Information (Country, Number, Date):

Patent: WO 8603634 A1 19860619

Application: WO 85US2443 19851210 (PCT/WO US8502443)

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International Patent Class: G06F-11:10

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 20935

English Abstract

An error detection and correction system includes a data transmission bus (196, 198) for transmitting data signals and error correction code (ECC) signals between a memory (28) and a processing unit (10). The ECC signals are in accordance with a modified Hamming code. An error detection and correction circuit (264) corrects single bit errors in data read from the memory (28). Also connected to the bus (196, 198) is a single bit error detection circuit (262) including a plurality of parity generators arranged to receive the data signals and selected ECC signals and adapted, when a single bit error is detected, to cause the blocking of a clock generator (94) thereby interrupting the operation of the processing unit (10). After a predetermined **time period** sufficient to enable the **error detection** and correction circuit (264) to correct the single bit error, operation of the clock generator (94) is resumed. The transmission bus includes a pair of individual buses (196, 198) and if both buses are utilized in a memory fetch operation, the error detection and correction circuit (264) operates successively on the data carried on the individual buses (196, 198).

French Abstract

Un systeme de detection et de correction d'erreurs comprend un bus de

transmission de donnees (196, 198) pour transmettre des signaux de donnees et des signaux de code de correction d'erreurs (CCE) entre une memoire (28) et une unite de traitement (10). Les signaux CCE sont conformes a un code Hamming modifie. Un circuit de detection et de correction d'erreurs (264) corrige des erreurs a un seul bit dans des donnees lues dans la memoire (28). Est egalement connecte au bus (196-198). Un circuit de detection d'erreurs a un seul bit (262) comprenant une pluralite de generateurs de parite disposes de maniere a recevoir les signaux de donnees et les signaux CCE choisis et adaptes, lorsqu'une erreur a un seul bit est detectee, pour provoquer le blocage d'un generateur a horloge (94), interrompant ainsi le fonctionnement de l'unite de traitement (10). Apres une periode determinee a l'avance, suffisante pour permettre au circuit de detection et de correction d'erreurs (264) de corriger l'erreur a un seul bit, le fonctionnement du generateur a horloge (94) reprend. Le bus de transmission comprend deux bus individuels (196, 198) et si les deux bus sont utilises dans une operation de recherche en memoire, le circuit de detection et de correction d'erreurs (264) agit successivement sur les donnees portees sur les bus individuels (196, 198).

Fulltext Availability:

Detailed Description

English Abstract

...clock generator (94) thereby interrupting the operation of the processing unit (10). After a predetermined **time period** sufficient to enable the **error detection** and correction circuit (264) to correct the single bit error, operation of the clock generator...

Detailed Description

... during the first memory cycle. While in ST01r the fetched data is put into the **EDAC** circuit 264 and is also used by the single **bit error detection** circuit 262 of Fig. 11.

In the **second memory cycle**, the state changes for ST01 at 511 to ST02 at 512 as shown in Fig...

...to the clock block logic circuit 426, as shown in Fig. 15B*
If a single **bit error** has been found by the single bit check circuit 418 or 420, as appropriate as...

...CLOCKS signal on conductor 428 as discussed in connection with Fig. 11. If a single **bit error** is found, the state changes from ST02 at 512 to ST03 at 513 for a...

...return the memory to idle for the start of another memory operation,
If no single **bit errors** were foundr the state changes from ST02 to ST00 as shown and the EDAC circuit 264 is checked for any double **bit errors** detected.

For a 64 bit fetch, the state changes from ST00 at 510 to ST12...

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File 111:TGG Natl.Newspaper Index(SM) 1979-2003/Oct 10
(c) 2003 The Gale Group
File 144:Pascal 1973-2003/Oct W1
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(c) 2003 EBSCO Publishing
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File 266:FEDRIP 2003/Aug
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? ds

Set	Items	Description
S1	6409643	TIME OR TIMING OR TIMER? ? OR CLOCK??? ? OR TEMPORAL
S2	2663519	MINUTE? ? OR SECOND? ?
S3	511172	S1:S2(3N) (INTERVAL? ? OR PHASE OR PHASES OR ZONE OR ZONES - OR PERIOD? ? OR CYCLE OR CYCLES OR SECTOR? ? OR DURATION? OR - STAGE OR STAGES)
S4	2575054	SAMPLE? OR SAMPLING?
S5	7770	ECC OR EDAC
S6	7715517	INVALID? OR MISTAK? OR FAIL? OR PROBLEM? OR FAULT? OR DEFE- CT? OR DEFICIEN? OR ABNORMA? OR FLAW? OR ABERRA? OR MALFUNCTI- ON?
S7	2413763	INOPERA? OR UNUSUAL OR DYSFUNCTION? OR DISFUNCTION? OR BUG? ? OR DETERIORAT? OR ATYPICAL? OR ERROR? ? OR DEVIA? OR IRREG- ULAR? OR CORRUPT?
S8	1250306	IMBALANC? OR EXCEPTION? ? OR DISTORT? OR DEGRAD? OR DISPAR- AT?
S9	489097	S6:S8(3N) (DETECT? OR DISCERN? OR FIND??? ? OR FOUND OR UNC- OVER? OR UN()COVER? OR CHECK? OR CHEQU? OR DIAGNOS? OR LOOK??? ? OR SEEK??? ?)
S10	999552	S6:S8(3N) (PROBE? ? OR PROBING OR SEARCH? OR ESTIMAT? OR EV- ALUAT? OR SURVEY? OR ANALYS? OR ANALYZ? OR ANALYT? OR ASSESS? OR EXAMIN? OR LOCAT? OR REVIEW? OR IDENTIFIC? OR IDENTIFIE? OR IDENTIFY?)
S11	81949	S6:S8(3N) (DISCRIMINAT? OR SCRUTIN? OR DIFFERENTIAT? OR SCR-

EEN? OR PINPOINT? OR PIN()POINT??? ? OR RECOGNIT? OR RECOGNIS?
OR RECOGNIZ?)

S12 288908 S6:S8(3N) (ASCERTAIN? OR INSPECT? OR DISTINGUISH? OR MONITO-
R? OR TRACK? OR TROUBLESHOOT? OR TROUBLE()SHOOT? OR SCAN OR S-
CANS OR SCANN??? ? OR TEST??? ?)

S13 5455 SELFTEST? OR SELFDIAGNOS? OR BIST

S14 965908 IC OR ICS OR INTEGRAT?? ?(1W) (CIRCUIT? OR OPTOELECTRONIC? -
OR OPTO()ELECTRONIC? ?) OR CHIP OR CHIPS OR MICROCIRCUIT? OR -
MICROELECTRONIC? ?

S15 156597 MICRO() (CIRCUIT? OR ELECTRONIC? ?) OR PRINTED(1W)CIRCUIT? -
OR MICROCHIP?

S16 269331 ASI OR ASIC OR VLSI OR VLSIC OR ULSI OR ULSIC OR VHSI OR V-
HSIC OR SOI OR SOIC OR MSI OR MSIC OR LSI OR LSIC

S17 24513 S3 AND (S5 OR S9:S13)

S18 1421 S17 AND S14:S16

S19 146 S18 AND S4

S20 124126 S4(3N) (DATA OR INPUT? OR SIGNAL? ? OR TRAFFIC? OR DATASTRE-
AM? OR STREAM?)

S21 64298 BER OR BERT OR (BIT OR BITS) (2N)ERROR?

S22 12 S18 AND S20

S23 46 S18 AND S21

S24 57 S22:S23

S25 7 S24/2002:2003

S26 50 S24 NOT S25

S27 44 RD (unique items)

S28 0 S18 AND MULTIBIT? ?(2N)ERROR?

? t27/7/all

27/7/1 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

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7420078 INSPEC Abstract Number: B2002-11-6120B-173

Title: Decoder-first code design

Author(s): Boutillon, E.; Castura, J.; Kschischang, F.R.

Author Affiliation: ENST, Paris, France

Conference Title: 2nd International Symposium on Turbo Codes and Related
Topics. Proceedings p.459-62

Publisher: Ecole Nationale Supérieure des Telecommun. Bretagne, Bretagne,
France

Publication Date: 2000 Country of Publication: France xviii+554 pp.

Material Identity Number: XX-2002-02421

Conference Title: 2nd International Symposium on Turbo Codes and Related
Topics. Proceedings

Conference Date: 4-7 Sept. 2000 Conference Location: Brest, France

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P); Theoretical (T); Experimental
(X)

Abstract: The natural approach for the design of an error correction
system is first to construct a code, then, define the hardware structure of
the decoder. Unfortunately, such a constructed code has very little chance
to be suited for a hardware implementation. This paper proposes to operate
the other way: in the first step an efficient hardware structure is chosen
and in the second step, a code is constructed that adequately fits this
structure. An example of such a methodology is exposed for a low density
parity check code. A cascable high speed (clock cycle equal to bit
rate) decoder architecture is presented and simulation results are given.
For an N=4096 LDPC code of rate 1/2, a bit error rate of 10/sup -4/ is
achieved respectively for SNRs of 2.63 dB (1 circuit), 2.3 dB (2 circuits)
and 2.05 dB (10 circuits). (7 Refs)

Subfile: B

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27/7/2 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

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7164748 INSPEC Abstract Number: B2002-03-6250-006

Title: A 0.6-2.5-GBaud CMOS tracked 3 * oversampling transceiver with dead-zone phase detection for robust clock /data recovery

Author(s): Yongsarn Moon; Deog-Kyoon Jeong; Gijung Ahn

Author Affiliation: Inter-University Semicond. Res. Center, Seoul Nat. Univ., South Korea

Journal: IEEE Journal of Solid-State Circuits Conference Title: IEEE J. Solid-State Circuits (USA) vol.36, no.12 p.1974-83

Publisher: IEEE,

Publication Date: Dec. 2001 Country of Publication: USA

CODEN: IJSCBC ISSN: 0018-9200

SICI: 0018-9200(200112)36:12L:1974:GCTO;1-N

Material Identity Number: I022-2002-001

U.S. Copyright Clearance Center Code: 0018-9200/01/\$10.00

Conference Title: 2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers

Conference Sponsor: IEEE Solid-State Circuits Soc.; IEEE San Francisco Sect.; Bay Area Council; Univ. PA

Conference Date: 5-7 Feb. 2001 Conference Location: San Francisco, CA, USA

Document Number: S0018-9200(01)09323-4

Language: English Document Type: Conference Paper (PA); Journal Paper (JP)

Treatment: Practical (P); Experimental (X)

Abstract: For generation of the multiphase clocks for a serializer, a wide-range multiphase delay-locked loop (DLL) is used in the transmitter to avoid the detrimental characteristics of a phase-locked loop (PLL), such as jitter peaking and accumulated phase error. A tracked 3 * oversampling technique with dead-zone phase detection is incorporated in the receiver for robust clock/data recovery in the presence of excessive jitter and intersymbol interference (ISI). Due to the dead-zone phase detection, phase adjustment is performed only on the tail portions of the transition histogram in the received data eye, thereby exhibiting wide pumping-current range, large jitter tolerance, and small phase error. A voltage-controlled oscillator (VCO), based on a folded starved inverter, shows about 50% less jitter than one with replica bias. The transceiver, implemented in 0.25- μ m CMOS technology, operates at 2.5 GBaud over a 10-m 150- Ω STP cable and at 1.25 GBaud over a 25-m cable with a bit error rate (BER) of less than 10^{-13} . (20 Refs)

Subfile: B

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27/7/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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7113572 INSPEC Abstract Number: B2002-01-2550R-002

Title: Development and characterization of an alpha particle low emissivity measurement system for semiconductor industry

Author(s): Sung Lee; Enman, C.; Mistry, A.; Carroll, B.; Sheridan, D.; Mathew, V.; Thomson, B.; Weeks, D.; Tucker, M.

Author Affiliation: Motorola Inc., Austin, TX, USA

Conference Title: Proceedings 2000 HD International Conference on

High-Density Interconnect and Systems Packaging (SPIE Vol.4217) p.455-60
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA
Publication Date: 2000 Country of Publication: USA xvi+617 pp.
ISBN: 0 930815 60 2 Material Identity Number: XX-2001-01667
Conference Title: 2000 HD International Conference on High-Density Interconnect and Systems Packaging
Conference Sponsor: SPIE; IMAPS - Int. Microelectron. & Packaging Soc.; CMP Media
Conference Date: 25-28 April 2000 Conference Location: Denver, CO, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: As technology lends itself to the creation of finer design geometries and lower voltage requirements, so too grows the potential for device upset, or soft failures, caused by alpha particles flipping the logic state of affected nodes. Alpha particles, which are high energy, highly charged particles, result from the decay of the naturally occurring radioisotopes uranium and thorium, and are both commonly found in **integrated circuit** manufacturing materials. Packaging, molding compounds, and die coat fillers, along with sputtering targets and Pb/Sn solder are all sources of alpha particles. DRAM manufacturers are aware of the advantages of using low alpha emission material. Using current industry standard detectors to measure alpha particle emission requires the creation of samples of the given material, which are counted for extended **periods of time**, due to the random nature of alpha emission events and the need for dependable statistics. However, this form of alpha counting, when applied to bulk material analysis, is very costly in terms of time. Using these same industry standard detectors, an adequate alternative method has been developed. The method recommends establishing a background emission signature derived by using an appropriate Poisson distribution on the measured data and supplementing the actual **samples** with simulated **data**. This method is more appropriate as the counts from the sample are indistinguishable from the detector background. Material that emits 0.02 count/cm/sup 2//hr or less is generally considered low alpha material. (7 Refs)
Subfile: B
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27/7/4 (Item 4 from file: 2)
DIALOG(R) File 2:INSPEC
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6455487 INSPEC Abstract Number: B2000-02-7250G-003
Title: Jitter measurement: pinning down timing at the leading edge
Author(s): Strassberg, D.
Journal: EDN (US Edition) vol.44, no.15 p.99-106
Publisher: Cahners Publishing,
Publication Date: 22 July 1999 Country of Publication: USA
CODEN: EDNEFD ISSN: 0012-7515
SICI: 0012-7515(19990722)44:15L:99:JMPD;1-Y
Material Identity Number: G340-1999-022
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P); Experimental (X)
Abstract: As **clock periods** shrink jitter that nobody used to notice on waveform edges is becoming a major cause of corrupted digital data. Attempting to quantify jitter on the basis of its effects (for example, with a **bit - error rate tester**) does not reveal as much about jitter sources as do direct measurements. Direct jitter measurements use **time - interval** analyzers, counter/ **timer** -based instruments, and (primarily real-time sampling) digital oscilloscopes. New all-digital techniques for

complex ASICs that contain PLLs can build the jitter measurement circuits onto the IC . (0 Refs)

Subfile: B

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27/7/5 (Item 5 from file: 2)

DIALOG(R)File 2:INSPEC

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5262382 INSPEC Abstract Number: A9611-9385-093, B9606-7710D-072

Title: Simultaneous measurement of pressure, temperature, and conductivity with counters

Author(s): Williams, A., III; Fraenkel, N.R.

Author Affiliation: Dept. of Appl. Ocean Phys. & Eng., Woods Hole Oceanogr. Instn., MA, USA

Conference Title: `Challenges of Our Changing Global Environment`. Conference Proceedings. OCEANS `95 MTS/IEEE (Cat. No.95CH35870) Part vol.1 p.626-30 vol.1

Publisher: IEEE, New York, NY, USA

Publication Date: 1995 Country of Publication: USA 3 vol. (xxxxiii+xxxvii+2103) pp.

ISBN: 0 933957 14 9 Material Identity Number: XX95-03103

Conference Title: `Challenges of Our Changing Global Environment`. Conference Proceedings. OCEANS `95 MTS/IEEE

Conference Sponsor: Marine Technol. Soc.; OES; IEEE

Conference Date: 9-12 Oct. 1995 Conference Location: San Diego, CA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: New Developments (N); Practical (P)

Abstract: Modular sensors of pressure, temperature, and conductivity with frequency outputs can be simultaneously sampled with counters. Power for the counters is inconsequential and there is no serious limit for counting period. Many sensors can be sampled simultaneously by simply adding counters. This is an old technique but complex sensing packages with low power, modular, frequency output sensors make it an attractive one. The number of stages of the counter, the stability of the sample interval, and the clocking of the serial shift register that moves the count to the logger are important considerations. Sample clock instabilities or timing errors must be detected and corrected and lost high order bits due to overscaling of the counters must be restored. With these considerations, modular frequency output sensors can be added to an underwater system for an incremental cost of one electrical penetration per sensor. (7 Refs)

Subfile: A B

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27/7/6 (Item 6 from file: 2)

DIALOG(R)File 2:INSPEC

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5211754 INSPEC Abstract Number: B9604-6250F-128

Title: Sensitivity of a DS CDMA system with long PN sequences to synchronization errors

Author(s): Sunay, M.O.; McLane, P.J.

Author Affiliation: Dept. of Electr. & Comput. Eng., Queen's Univ., Kingston, Ont., Canada

Conference Title: ICC `95 Seattle. Communications - Gateway to Globalization. 1995 IEEE International Conference on Communications (Cat. No.95CH35749) Part vol.2 p.1029-35 vol.2

Publisher: IEEE, New York, NY, USA
 Publication Date: 1995 Country of Publication: USA 3 vol. xxviii+1985 pp.
 ISBN: 0 7803 2486 2 Material Identity Number: XX95-02234
 U.S. Copyright Clearance Center Code: 0 7803 2486 2/95/\$4.00
 Conference Title: Proceedings IEEE International Conference on Communications ICC '95
 Conference Sponsor: IEEE Commun. Soc.; IEEE Seattle Sect
 Conference Date: 18-22 June 1995 Conference Location: Seattle, WA, USA
 Language: English Document Type: Conference Paper (PA)
 Treatment: Theoretical (T)
 Abstract: Use of direct sequence code division multiple access (DS CDMA) has been the object of much attention in the research and development of a multi-service personal communications network. The performance of such a system is usually given in terms of the **bit error** rate as a function of the number of active users for a given signal to noise ratio. We have investigated the degradation in the performance of a BPSK modulated, bi-phase spread DS CDMA system due to synchronization errors. A Fourier series approach has been used to find an infinite series representation for the probability of error when both **chip timing** and carrier **phase errors** are present. The **analysis** requires the characteristic functions of both the multiple access interference and self interference and these functions have been expressed in terms of the special functions of mathematical physics. Computation of the infinite series is very fast as a whole **bit error** curve can be generated in minutes on a Sparc IPX workstation. The infinite series is also compared with the standard Gaussian approximation and an alternative Gaussian approximation found in the literature. The series is then used to assess the reduction in system capacity when synchronization errors are present in the system. We have expressed this degradation in the system performance as an effective processing gain reduction. (11 Refs)
 Subfile: B
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27/7/7 (Item 7 from file: 2)
 DIALOG(R)File 2:INSPEC
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4764925 INSPEC Abstract Number: B9410-6270-002, C9410-3390-171
Title: Real time DSP based underwater communications
 Author(s): Barroso, V.; Geada, P.; Gomes, J.P.
 Author Affiliation: ISR Complexo I, Inst. Superior Tecnico, Lisbon, Portugal
 Part vol.2 p.1584-93 vol.2
 Publisher: DSP Associates, Newton, MA, USA
 Publication Date: 1993 Country of Publication: USA 2 vol. 1675 pp.
 Conference Title: Proceedings of the Fourth International Conference on Signal Processing Applications and Technology. ICSPAT '93
 Conference Date: 28 Sept.-1 Oct. 1993 Conference Location: Santa Clara, CA, USA
 Language: English Document Type: Conference Paper (PA)
 Treatment: Theoretical (T)
 Abstract: This paper presents a communications system designed for use between an autonomous underwater vehicle (AUV) and its surface base station, but well suited for many other applications where reliable real time underwater data communication is required. Digital communications in underwater acoustic channels present some problems such as heavy intersymbol interference (ISI) due to multipath propagation, rapidly changing channel characteristics and Doppler effects. In order to achieve low **bit error** rate, high performance filtering is required. The paper

discusses several techniques which are combined to form a powerful equalization structure-decision-feedback (DFE) and fractionally-spaced (FSE) equalization, recursive least squares (RLS Kalman) filtering, and joint estimation of equalizer coefficients and synchronization parameters (carrier **phase** and symbol **timing**). A preliminary discussion involving an all-digital, real time implementation on a Motorola DSP 56001 digital signal processor is presented. Fast Kalman type **estimation**, solving the RLS **problem** with a reduced number of operations proved to be suited for real time operation. The recently developed "modular fast transversal filter" algorithm is used, avoiding matrix operations on a DSP, while retaining the multichannel formulation needed for DFE and FSE. Experimental results obtained with both simulated and real data are discussed, showing the efficiency of the system. (12 Refs)

Subfile: B C

27/7/8 (Item 8 from file: 2)

DIALOG(R)File 2:INSPEC

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4622483 INSPEC Abstract Number: B9404-6250G-033

Title: A burst mode all-digital high-speed clock recovery circuit and block clock recovery scheme

Author(s): Matsumoto, Y.; Morikura, M.; Kato, S.

Author Affiliation: NTT Radio Commun. Syst. Labs., Yokosuka, Japan

Journal: Electronics and Communications in Japan, Part 1 (Communications) vol.76, no.7 p.70-80

Publication Date: July 1993 Country of Publication: USA

CODEN: ECJCED ISSN: 8756-6621

U.S. Copyright Clearance Center Code: 8756-6621/93/0007-0070

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P); Theoretical (T)

Abstract: This paper is focused on an all-digital implementation of the high-speed burst mode demodulator for time-division multiple access (TDMA) satellite communication. A clock recovery scheme in a preamble-less burst recovery demodulator is considered. A burst clock recovery scheme is proposed which can be operated at a speed twice higher than the symbol rate. The deterioration due to the error in the **clock phase** estimation in the burst clock recovery scheme is regarded as a stochastic process, and the effect of the burst signal on the **bit error** rate is **evaluated** by computer simulation. It is shown, as an example, that when the burst clock recovery scheme is applied to the TDMA satellite communication with a burst length of 800 symbols and transmission filter roll-off factor of 0.4, the burst probability is 1×10^{-6} times/burst for the degradation of 0.2 dB of $E_{\text{sub}}/N_{\text{sub}}$. In other words, the proposed system affects only slightly the burst loss probability required in the TDMA system. (9 Refs)

Subfile: B

27/7/9 (Item 9 from file: 2)

DIALOG(R)File 2:INSPEC

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4509291 INSPEC Abstract Number: B9312-1265B-030, C9312-5210-013

Title: A study of the effects of transient fault injection into a 32-bit RISC with built-in watchdog

Author(s): Ohlsson, J.; Rimen, M.; Gunneflo, U.

Author Affiliation: Chalmers Univ. of Technol., Goteborg, Sweden

Conference Title: Digest of Papers. The 1992 IEEE Workshop on Fault-Tolerant Parallel and Distributed Systems (Cat. No.92TH0449-9) p.

316-25

Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1992 Country of Publication: USA viii+233 pp.
ISBN: 0 8186 2870 7

U.S. Copyright Clearance Center Code: 0 8186 2870 7/92\$03.00

Conference Sponsor: IEEE

Conference Date: 6-7 July 1992 Conference Location: Amherst, MA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: This paper presents an **error - detecting** 32-bit RISC, designed in a 1.2 μ m CMOS technology, with an on-chip watchdog using embedded signature monitoring. It is **evaluated** through simulation-based **fault** injection, using a register level model written in VHDL. A **chip** area increase of 4.7% was caused by the watchdog. Two application programs were executed to study workload dependencies. The insertion of watchdog instructions resulted in a memory overhead of between 13% and 25% as well as a performance overhead of between 9% and 19%. A total of 2779 faults were injected into the processor during execution of the application programs. Only 23% of these resulted in effective **errors**. A minimum **detection** coverage of 95% was reached for effective errors classified as control flow errors with a median latency of one **clock cycle**. Few effective data errors, between 22% and 50%, were detected. (22 Refs)

Subfile: B C

27/7/10 (Item 10 from file: 2)

DIALOG(R) File 2:INSPEC

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04095435 INSPEC Abstract Number: B9204-1265B-018, C9204-5120-008

Title: A 64 b CMOS mainframe execution unit macrocell with error detecting circuit

Author(s): Hayashi, T.; Doi, T.; Yamagishi, M.; Koide, K.; Ishiyama, A.; Hiramatsu, M.; Yamagiwa, A.

Author Affiliation: Central Res. Lab., Hitachi Ltd., Kokubunji, Japan

Journal: IEICE Transactions vol.E74, no.11 p.3775-9

Publication Date: Nov. 1991 Country of Publication: Japan

CODEN: IEITEF ISSN: 0917-1673

Language: English Document Type: Journal Paper (JP)

Treatment: Applications (A); Practical (P)

Abstract: A 64 b CMOS mainframe execution unit macrocell with **error detecting** circuits is proposed. The conventional techniques to maintain high reliability have been the parity checking and the duplication of the ALU (Arithmetic Logic Unit). However, the required time for generating the parity from the sum output of the ALU has been undesirable for high-speed operation. In order to achieve a short ALU delay time, a parity predicting logic structure is newly adopted. By utilizing this structure a one-bit **error detecting** function is integrated without duplicating every ALU circuit. A novel CMOS precharged circuit is also developed to shorten the time required to precharge the whole circuit. When the number of circuit stages is reduced, the precharge time as well as the delay **time** restricts the ALU **cycle time**. This new circuitry solves the precharging time accumulation problem in the conventional circuits. A 64 b BCD ALU adopting this technology has been designed and fabricated. The parity predict architecture and the high-speed-precharge circuit have been effective in reducing the delay time by 23% and the precharge time by 42%. A 30% faster **cycle time** has been achieved with a small increase (4%) in ALU area. The execution unit macrocell, which includes the ALU described above, contains 45 k transistors and its area is 4.3 mm*4.1 mm using the 0.8 μ m CMOS triple metal layer technology. (6 Refs)

Subfile: B C

27/7/11 (Item 11 from file: 2)

DIALOG(R)File 2:INSPEC

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03976029 INSPEC Abstract Number: B91062266, C91057584

Title: A 10 b 15 MHz recycling two-step A/D converter

Author(s): Song, B.-S.; Tompsett, M.F.

Author Affiliation: Illinois Univ., Urbana, IL, USA

Conference Title: 1990 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. (Cat. No.90CH2824-1) p.158-9, 289

Publisher: IEEE, New York, NY, USA

Publication Date: 1990 Country of Publication: USA 336 pp.

U.S. Copyright Clearance Center Code: 0193-6530/90/0000-0158\$1.00

Conference Sponsor: IEEE; Bar Area Council; Univ. Pennsylvania

Conference Date: 14-16 Feb. 1990 Conference Location: San Francisco, CA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: A fully differential CMOS videorate converter whose linearity relies on a binary-weighted capacitor array known to exhibit a 10-b linearity is described. The recycling analog-to-digital converter (ADC) does not have the sampling error found in other two-step or multistep pipelined architectures because it requires only one input sampling per conversion. A single-ended schematic of a digitally corrected ADC is shown. One feature of this architecture is the multiple role of a capacitor-array multiplying digital-to-analog converter (MDAC). One MDAC replaces three functional blocks in a standard two-step architecture: a sample-and-hold amplifier, a residue amplifier, and a DAC. As a result, the proposed ADC does not require precision components other than an MDAC. One conversion is finished in three clock phases. (4 Refs)

Subfile: B C

27/7/12 (Item 12 from file: 2)

DIALOG(R)File 2:INSPEC

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02678594 INSPEC Abstract Number: B86035916

Title: High speed Manchester decoding using GaAs D-MESFET ICs

Author(s): Gianisis, D.A.; Prince, J.S.; Kwiat, J.J.

Author Affiliation: General Electric Co., Binghamton, NY, USA

Conference Title: GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. Technical Digest 1985 (Cat. No.85CH2182-4) p.83-6

Publisher: IEEE, New York, NY, USA

Publication Date: 1985 Country of Publication: USA 210 pp.

U.S. Copyright Clearance Center Code: CH2182-4/85/0000-0083\$01.00

Conference Sponsor: IEEE

Conference Date: 12-14 Nov. 1985 Conference Location: Monterey, CA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P); Experimental (X)

Abstract: The use of digital GaAs ICs in the receiver portion of a bus interface unit (BIU) that is being developed to connect to an electrical high-speed data bus (HSDB) is examined. The receiver includes a GaAs Manchester decoder and 100K ECL circuits for serial-to-parallel data conversion. The GaAs chip set decodes 100-Mb/s Manchester II encoded

data. The cell array has been designed and fabricated. Functional testing of the cell array has shown working parts on the first iteration with a 20% yield. Incoming asynchronous Manchester II data is oversampled and processed using a 1.25-ns **cycle time**. The cell array outputs differential non-return-to-zero (NRZ) data and clock along with an **error detect bit**. (1 Refs)

Subfile: B

27/7/13 (Item 13 from file: 2)

DIALOG(R)File 2:INSPEC

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02556077 INSPEC Abstract Number: B85061285, C85049947

Title: A 4-byte 18 ns ECC for hard and soft correction

Author(s): Glaise, R.; Lehouchu, J.

Author Affiliation: 'Centro d'Etudes et de Recherches', Lagaude, France

Conference Title: ESSCIRC '84. Tenth European Solid-State Circuits Conference p.157-60

Publisher: CEP Consultants, Edinburgh, UK

Publication Date: 1984 Country of Publication: UK x+283 pp.

Conference Sponsor: EUREL; IEE; IEEE; R. Soc. Edinburgh

Conference Date: 19-21 Sept. 1984 Conference Location: Edinburgh, UK

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: High density random access memory modules are subject to the so-called 'soft error'. The **ECC** module described is capable of correcting any single **bit error** within a word and detects all combinations of 2-**bit errors**. Moreover, it is possible to operate the device both in 'Normal' and 'Invert' modes allowing the implementation of an 'Invert and Retry' cycle. Such a **cycle** is executed each **time** a 2 **bit error** is encountered. The use of such a device improves the hard failure rate by at least one order of magnitude and permits to be absolutely insensitive to the soft or intermittent errors. The **ECC** code has been chosen so that the data field to be checked by the parity checkers are minimum. Only 3-bit combinations are used. The access time of the main memory sets the throughput of the processor and it is especially important not to impact it when the memory is equipped with an **ECC**. To do so, the EEC is implemented with an ECL type of circuit on a master slice basic gate which is obviously a NOR gate with inverted and non-inverted outputs. (2 Refs)

Subfile: B C

27/7/14 (Item 14 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

02176690 INSPEC Abstract Number: B84006802

Title: GaAs integrated circuits for error-rate measurement in high-speed digital transmission systems

Author(s): Liechti, C.A.; Joly, R.; Namjoo, M.

Author Affiliation: Hewlett-Packard Labs., Palo Alto, CA, USA

Journal: IEEE Journal of Solid-State Circuits vol.SC-18, no.4 p. 402-8

Publication Date: Aug. 1983 Country of Publication: USA

CODEN: IJSCBC ISSN: 0018-9200

U.S. Copyright Clearance Center Code: 0018-9200/83/0800-0402\$01.00

Language: English Document Type: Journal Paper (JP)

Treatment: Applications (A); Practical (P)

Abstract: A high-speed GaAs **MSI** PRBS generator and an **error detector**

have been built, tested, and applied to **bit - error** ratio measurements in a fiber-optic transmission link. The generator produces a 1023 bit sequence at 2 Gbit/s data rate. The detector compares, bit-by-bit, the input data with a locally regenerated sequence. With a 2 GHz clock, the direct-coupled generator/detector combination, without an optical link, exhibits less than one error in 10/sup 14/ **clock cycles**. The complete fiber-optic link test system incorporates a 1 km multimode fiber, operates at 1.9 Gbits/s, and exhibits a **bit - error** ratio below 10/sup -12/. (25 Refs)

Subfile: B

27/7/15 (Item 15 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

02016555 INSPEC Abstract Number: B83017754, C83013389

Title: 32-bit EDAC chips fix single-bit errors efficiently

Author(s): Greer, W.T.; Breuninger, R.

Author Affiliation: Texas Instruments Inc., Dallas, TX, USA

Journal: Electronic Design vol.31, no.1 p.269-74

Publication Date: 6 Jan. 1983 Country of Publication: USA

CODEN: ELODAW ISSN: 0013-4872

Language: English Document Type: Journal Paper (JP)

Treatment: Applications (A); Practical (P)

Abstract: Describes how **error detection** and **error correction chips** can be designed into RAMs. There is some **cycle - time** penalty, but these devices can keep pace with the fastest RAMs and can increase tenfold the system mean time between failure. The authors emphasise the use of the SN54/74ALS632-635 family of **chips**. (0 Refs)

Subfile: B C

27/7/16 (Item 16 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

01999831 INSPEC Abstract Number: B83012233

Title: A GaAs MSI pseudo-random bit-sequence generator and error detector operating at 2 Gbits/s data rate

Author(s): Joly, R.; Liechti, C.; Namjoo, M.

Author Affiliation: Hewlett-Packard Labs., Palo Alto, CA, USA

Conference Title: GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. Technical Digest 1982 p.33-5

Publisher: IEEE, New York, NY, USA

Publication Date: 1982 Country of Publication: USA 190 pp.

U.S. Copyright Clearance Center Code: CH1764-0/82/0000-0033\$00.75

Conference Sponsor: IEEE

Conference Date: 9-11 Nov. 1982 Conference Location: New Orleans, LA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P)

Abstract: A high-speed GaAs PRBS generator and an **error detector IC** have been built, tested and applied to **bit - error** -rate measurements in a fibre-optic transmission link. The generator produces a 1023 bit sequence at 2 Gb/s data rate. The detector regenerates the original PRBS from a series of error-free input data. It then compares, bit-by-bit, the regenerated sequence with the subsequent input data. With a 2 GHz clock, the basic generator/detector combination exhibits less than one error in 10/sup 14/ **clock cycles**. (4 Refs)

Subfile: B

27/7/17 (Item 1 from file: 6)

DIALOG(R)File 6:NTIS

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1566684 NTIS Accession Number: N91-13622/6

Detection of Multiple- Bit Errors from Single-Ion Tracks in Integrated Circuits

(Patent Application)

Zoutendyk, J. A.

National Aeronautics and Space Administration, Pasadena, CA. Pasadena Office.

Corp. Source Codes: 064668001; ND894694

Report No.: PAT-APPL-7-555 865

Filed 23 Jul 90 17p

Languages: English Document Type: Patent

Journal Announcement: GRAI9111; STAR2905

This Government-owned invention available for U.S. licensing and, possibly, for foreign licensing. Copy of application available NTIS. Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC N03/MF A01

Country of Publication: United States

Contract No.: NAS7-918

A **error detector** and imaging system for multiple-bit errors from single-ion tracks in integrated circuits distinguishes between multiple bit errors caused by ion tracks which do not strike charge collection junctions having substantial capacitance and those that do on the basis of the sensitivity of the errors to changes in VDD. Data which do not occur during the **time interval** between successive read cycles, which do not occur at integral multiples of the read clock, whose recorded time tags are not greater than those of previous data or whose recorded address tags are not greater than those of previous data are discarded as bad data before further processing and display.

27/7/18 (Item 1 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

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05997111 E.I. No: EIP02056842575

Title: A 0.6-2.5-GBaud CMOS tracked 3 multiplied by oversampling transceiver with dead-zone phase detection for robust clock /data recovery

Author: Moon, Yongsam; Jeong, Deog-Kyoon; Ahn, Gijung

Corporate Source: Seoul National University ISRC, Seoul 151-742, South Korea

Source: IEEE Journal of Solid-State Circuits v 36 n 12 December 2001. p 1974-1983

Publication Year: 2001

CODEN: IJSCBC ISSN: 0018-9200

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical); X; (Experimental)

Journal Announcement: 0202W1

Abstract: For generation of the multiphase clocks for a serializer, a

wide-range multiphase delay-locked loop (DLL) is used in the transmitter to avoid the detrimental characteristics of a phase-locked loop (PLL), such as jitter peaking and accumulated phase **error**. A **tracked** 3 multiplied by oversampling technique with dead-zone phase detection is incorporated in the receiver for robust clock/data recovery in the presence of excessive jitter and intersymbol interference (ISI). Due to the dead-zone phase detection, phase adjustment is performed only on the tail portions of the transition histogram in the received data eye, thereby exhibiting wide pumping-current range, large jitter tolerance, and small phase error. A voltage-controlled oscillator (VCO), based on a folded starved inverter, shows about 50% less jitter than one with replica bias. The transceiver, implemented in 0.25- μ m CMOS technology, operates at 2.5 GBaud over a 10-m 150- Ω STP cable and at 1.25 GBaud over a 25-m cable with a **bit error** rate (BER) of less than 10^{-13} . 20 Refs.

27/7/19 (Item 2 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

05926794 E.I. No: EIP01436704048

Title: A scalable 32Gb/s parallel data transceiver with on-chip timing calibration circuits

Author: Yang, K.; Lin, T.; Ke, Y.

Corporate Source: HotRail Inc., San Jose, CA, United States

Conference Title: 2000 IEEE International Solid-State Circuits Conference 47th Annual ISSCC

Conference Location: San Francisco, CA, United States Conference Date: 20000207-20000209

E.I. Conference No.: 58583

Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 2000. p 258-259 (IEEE cat n 00CH37056)

Publication Year: 2000

CODEN: DTPCDE ISSN: 0193-6530

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 0111W1

Abstract: A scalable 32 Gb/s parallel data transceiver was analyzed with on-chip timing calibration circuits. These circuits perform data de-skewing and timing optimization. The clock phase detector was used to determine the phase relationship between the core clock and the received clock. The **bit error** rate (BER) test was also conducted by HP 81200 data generator and analyzer with random patterns. (Edited abstract) 2 Refs.

27/7/20 (Item 3 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

05926705 E.I. No: EIP01436703959

Title: A 14b 20MSample/s CMOS pipelined ADC

Author: Chen, H.-S.; Bacrania, K.; Song, B.-S.

Corporate Source: Intersil Corp., Melbourne, FL, United States

Conference Title: 2000 IEEE International Solid-State Circuits Conference 47th Annual ISSCC

Conference Location: San Francisco, CA, United States Conference Date: 20000207-20000209

E.I. Conference No.: 58583

Source: Digest of Technical Papers - IEEE International Solid-State

Circuits Conference 2000. p 46-47 (IEEE cat n 00CH37056)

Publication Year: 2000

CODEN: DTPCDE ISSN: 0193-6530

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 0111W1

Abstract: A 14b 20M Sample per second CMOS pipelined analog to digital converter (ADC) is described. This ADC uses an extra **clock phase** for averaging the capacitor **errors**. A combination of **look-ahead** decision and digital correction concepts was utilized in this ADC. This allows residual amplifiers and comparators to operate within a full **clock phase**. Twelve pipelined **stages** are cascaded along with a 2b flash at the end. (Edited abstract) 3 Refs.

27/7/21 (Item 4 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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05407546 E.I. No: EIP99104866052

Title: Modeling and simulation of noise in analog/mixed-signal communication systems

Author: Demir, Alper; Roychowdhury, Jaijeet

Corporate Source: Bell Lab, Murray Hill, UT, USA

Conference Title: Proceedings of the 1999 21st IEEE Annual Custom Integrated Circuits Conference, CICC '99

Conference Location: San Diego, CA, USA Conference Date: 19990516-19990519

Sponsor: IEEE Solid States Circuits Society

E.I. Conference No.: 55491

Source: Proceedings of the Custom Integrated Circuits Conference 1999. p 385-392

Publication Year: 1999

CODEN: PCICER ISSN: 0886-5930 ISBN: 0-7803-5444-3

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical)

Journal Announcement: 9912W2

Abstract: Noise in analog and mixed-signal electronic systems is an undesired but unavoidable excitation on the circuit. Its analysis and modeling is relatively straightforward in linear analog circuits, such as amplifiers. For such circuits, the SPICE AC noise analysis is, most of the time, adequate for noise performance characterization. However, for communication circuits, where nonlinearities and frequency translation are inherent, SPICE AC noise analysis is not adequate. Recently, there has been a great deal of activity, both in the design and CAD communities, to develop noise analysis techniques and tools to treat problems with nonlinear and frequency translation effects. In this tutorial, we first present the basic concepts and fundamental techniques used in noise analysis and modeling both for linear and nonlinear circuits. Then, we concentrate on some specific noise modeling and **analysis problems** in mixed-signal communication system design, e.g., mixers, **phase** noise and **timing** jitter, digital switching interference, etc. (Author abstract) 54 Refs.

27/7/22 (Item 5 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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05050788 E.I. No: EIP98074264256

Title: 300 Mb/s BiCMOS EP4 read channel for magnetic hard disks

Author: Leung, M.; Chiu, J.; VanScheik, B.; Wang, L.; Fu, L.; Rosky, D.; Stoiber, S.; Huntington, A.; Liu, C.; Loh, S.-C.; Hsiung, C.; Zhang, J.; Fukahori, K.; Hutchinson, D.; Lee, T.-L.

Corporate Source: Silicon Systems Inc, San Jose, CA, USA

Conference Title: Proceedings of the 1998 IEEE 45th International Solid-State Circuits Conference, ISSCC

Conference Location: San Francisco, CA, USA Conference Date: 19980205-19980207

Sponsor: IEEE

E.I. Conference No.: 48558

Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1998. IEEE, Piscataway, NJ, USA, 98CH36156. p 378-379, 467 PAPER SP 24.1

Publication Year: 1998

CODEN: DTPCDE ISSN: 0193-6530

Language: English

Document Type: CA; (Conference Article) Treatment: G; (General Review); X; (Experimental)

Journal Announcement: 9808W4

Abstract: A 300 Mb/s read channel **integrated circuit (IC)** is fabricated in 0.8 μ m BiCMOS and majority of the signal processing is carried out in the analog **sampled - data** domain. The key circuit block is an 8-state time interleaved EP4 (extended partial response) Viterbi trellis **detector**. The **bit error** rate performance show ideal performance gain over a PR4 channel. The sync pattern detection of the channel uses two 17 b sync patterns. **Detection** of the non- **fault** -tolerant SB2 is performed by a simple AND operation, and **fault** -tolerant **detection** of SB1 is carried out using analog current summing for its small Si area and low power dissipation. The current summing and comparison operation is rapid, allowing each incoming work in a single **clock cycle** to be checked. 4 Refs.

27/7/23 (Item 6 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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05009463 E.I. No: EIP98054179581

Title: Low-power VLSI architecture for the Viterbi decoder

Author: Ju, Wann-Shyang; Shieh, Ming-Der; Sheu, Ming-Hwa

Corporate Source: Natl Yunlin Univ of Science & Technology, Yunlin, Taiwan

Conference Title: Proceedings of the 1997 40th Midwest Symposium on Circuits and Systems. Part 2 (of 2)

Conference Location: Sacramento, CA, USA Conference Date: 19970803-19970806

Sponsor: IEEE

E.I. Conference No.: 48277

Source: Midwest Symposium on Circuits and Systems v 2 1997. IEEE, Piscataway, NJ, USA, 97CB36010. p 1201-1204

Publication Year: 1997

CODEN: MSCSDL

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 9807W1

Abstract: This paper presents a **VLSI** architecture for the Viterbi decoder toward reducing average power dissipation based on the modified T-algorithm and the radix-2 butterfly module. Simulation results show that on the average, more than half of states at each **time stage** are not

needed to be processed for the (4,1,6) convolutional code at bit error probability P/b less than equivalent to 10^{**2} . Therefore, significant power reduction can be achieved by reducing the total number of path metric computations and eliminating waste memory read/write operations. Based on the TSMC 0.6 μ m SPDM process and the Compass cell library, the resulting core size is $2761 \times 2996 \mu m^{**2}$. (Author abstract) 14 Refs.

27/7/24 (Item 7 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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04928687 E.I. No: EIP98024045133

Title: Decorrelator detection for quasi-synchronous multicarrier CDMA

Author: Iltis, Ronald A.

Corporate Source: Univ of California, Santa Barbara, CA, USA

Conference Title: Proceedings of the 1997 MILCOM Conference. Part 2 (of 3)

Conference Location: Monterey, CA, USA Conference Date: 19971103-19971105

Sponsor: IEEE

E.I. Conference No.: 47731

Source: Proceedings - IEEE Military Communications Conference MILCOM v 2 1997. IEEE, Piscataway, NJ, USA, 97CB36134. p 862-866

Publication Year: 1997

CODEN: PMICET

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 9804W1

Abstract: A new multicarrier CDMA receiver is proposed for the reverse channel (mobiles to base) of a quasi-synchronous CDMA (QS-CDMA) system, which uses a decorrelator to demodulate the signal in each carrier. The advantage of the multi-carrier CDMA system for quasi-synchronous operation is that the **timing uncertainty interval** can be progressively decreased by increasing the number of carriers and bits in the serial-to-parallel buffer. It has previously been shown that a modified decorrelator based on **chip** matched filter samples completely rejects undesired users with delays falling in the quasi-synchronous uncertainty interval. Here, it is also shown that the decorrelator rejects adjacent carrier undesired users, in contrast to the case of a system employing conventional matched filtering. Analytic **BER** results are presented for the decorrelator-based multicarrier CDMA system, under the conditions of Rayleigh frequency non-selective fading in each sub-band. (Author abstract) 7 Refs.

27/7/25 (Item 8 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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04383986 E.I. No: EIP96043141032

Title: Digital ultrafast carrier recovery for interactive transmission systems

Author: Brown, Chuck; Do, Gary; Feher, Kamilo

Corporate Source: Univ of California, Davis, LA, USA

Source: IEEE Transactions on Consumer Electronics v 42 n 1 Feb 1996. p 132-139

Publication Year: 1996

CODEN: ITCEDA ISSN: 0098-3063

Language: English

Document Type: JA; (Journal Article) Treatment: A; (Applications)

Journal Announcement: 9606W3

Abstract: An ultrafast, all-digital method for phase synchronization and coherent carrier recovery is presented for time division multiple access (TDMA) and code division multiple access (CDMA) burst data communication systems. A new adaptive phase tracking (APT) method, presented and analyzed in this paper, uses a hard-limited IF signal in a feed forward configuration for carrier phase detection and recovery. A novel new technique of phase window filtering is presented as a means to combat noise induced phase errors, and improved the performance of a digital controlled phase shift oscillator by 7 dB. Experimental measurements show APT provides robust **bit error rate (BER)** performance within 1 dB of the theoretical binary phase shift keyed (BPSK) and tenths of dBs of an ideal hard wired clock. APT achieves acquisition within one- to four-bits - 5 to 10 times faster than present requirements. A low power, low cost single **chip** fast carrier synchronization and demodulation solution for QPSK, GMSK and GSM compatible OQPSK and Feher's quadrature phase shift keyed (FQPSK) and binary phase shift keyed (FBPSK) systems left bracket 10 right bracket are also presented. (Author abstract) 11 Refs.

27/7/26 (Item 9 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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04346020 E.I. No: EIP96023022403

Title: 10Gb/s ATM data synchroniser

Author: Wong, Thomas Y.K.; Sitch, John; McGarry, Steve

Corporate Source: BNR, Ottawa, Ont, Can

Conference Title: Proceedings of the 17th Annual IEEE Gallium Arsenide Integrated Circuit Symposium

Conference Location: San Diego, CA, USA Conference Date: 19951029-19951101

Sponsor: IEEE

E.I. Conference No.: 44292

Source: GaAs IC Symposium Technical Digest - GaAs IC Symposium (Gallium Arsenide Integrated Circuit) 1995. IEEE, Piscataway, NJ, USA, 95CH35851. p 49-51

Publication Year: 1995

CODEN: TDGSEE

Language: English

Document Type: CA; (Conference Article) Treatment: A; (Applications)

Journal Announcement: 9604W1

Abstract: A data synchronizer based on an analog controlled data delay driven by a **clock** to data **phase** detector is reported. Fabricated in HRT it runs at 10 Gb/s with 200 ps delay range. Testing has shown that offsets can occur between the 'recenter' voltage and the middle of the delay control range, so a second generation design, currently in processing, has a recenter trim control. It also has a slightly increased delay range to improve performance margins. Notwithstanding the somewhat limited circumstances under which this **chip** can be used, it is a worthwhile addition to the devices available to systems designers. 3 Refs.

27/7/27 (Item 10 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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03702407 E.I. No: EIP93091067576

Title: Jitterreduced digital timing recovery for multilevel PAM and QAM

systems

Author: Lankl, B.; Sebald, G.
Corporate Source: Siemens AG
Conference Title: 1993 IEEE International Conference on Communications
Conference Location: Geneva, Switz Conference Date: 19930523-19930526
Sponsor: IEEE Communications Society; IEEE Switzerland Section
E.I. Conference No.: 18808
Source: IEEE International Conference on Communications 1993 IEEE Int
Conf Commun 1993. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p
804-810

Publication Year: 1993
ISBN: 0-7803-0951-0
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); T
; (Theoretical)
Journal Announcement: 9310W5

Abstract: In multilevel PAM/QAM systems, e.g. digital radio, there is a strong demand for a reliable and precise **timing phase** provided by the **timing** recovery circuit. This is much more true in case of a sharp pulseshaping filter which leads to a drastically increased sensitivity of the system performance (i.e. **BER** -curve, signatures) against **timing phase** deviations. These deviations from the correct **timing phase** or sampling **phase**, respectively, due to temperature drift, aging and misalignment can completely be overcome by using a digital **timing phase** detector which includes the sampling unit and is ideally suited for state of the art **VLSI** -technology. In addition to the increased sensitivity of the radio system due to **timing phase** deviations there are higher demands in terms of permissible phase jitter if the modulation scheme is extended, especially if small rolloff factors are used for pulseshaping. Reducing **timing phase** jitter further by narrowing of the timing recovery loop bandwidth decreases the ability of tracking the time variant radio channel. To avoid this drawback the only way to improve **timing phase** jitter which is pattern dependent is to use some signal processing means. Only by this means the accumulated jitter in repeater chains can be kept small. The solution which will be presented in the paper offers a theoretically jitterfree phase detector even in the case of noncoherent demodulation. Also in practical applications with reduced complexity a remarkable amount of jitter reduction in the order of greater than 15 dB is achieved. Furthermore solutions to improve the behaviour of the timing recovery in case of linear channel distortions are given. (Author abstract)
9 Refs.

27/7/28 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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06187280 Genuine Article#: YA508 Number of References: 20
Title: A new symbol timing and carrier frequency offset estimation
algorithm for noncoherent orthogonal M-CPFSK
Author(s): Caire G (REPRINT) ; Elia C
Corporate Source: POLITECN TURIN, DIPARTIMENTO ELETTRON/I-10129
TURIN//ITALY/ (REPRINT); EUROPEAN SPACE TECHNOL CTR, EUROPEAN SPACE
AGCY/NL-2200 AG NOORDWIJK//NETHERLANDS/
Journal: IEEE TRANSACTIONS ON COMMUNICATIONS, 1997, V45, N10 (OCT), P
1314-1326
ISSN: 0090-6778 Publication date: 19971000
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST,
NEW YORK, NY 10017-2394
Language: English Document Type: ARTICLE

Abstract: We present a new joint symbol timing and carrier frequency offset estimation algorithm for noncoherent orthogonal continuous-phase M-ary frequency-shift keying (M-CPFSK). Our algorithm performs nondata-aided feedforward processing of finite-length observations, and it is suited for an all-digital modem implementation based on a DSP or an ASIC professor, The algorithm exploits phase continuity of M-CPFSK in order to generate both a spectral component at the carrier frequency offset and a timing error signal, This is obtained without nonlinear transformations of the received signal involving noise x noise products, Thus, our algorithm can operate at a very low input signal-to-noise ratio.

We discuss the operating range of our algorithm, and we show that no additional overhead (training sequence) in excess of the standard overhead of FDMA/TDMA packet transmission is required to resolve timing and frequency ambiguities. Moreover, we show that by differentially preceding the transmitted symbols, it is possible to eliminate automatically frequency ambiguities, at the price of a slight increase in the **bit - error** rate. An approximate mean-square **error analysis** of the **estimators** and simulation results prove that our algorithm provides good performance, even with a relatively short observation block length and large carrier frequency offset. Computer simulations show also that our algorithm is extremely robust to phase noise, These features make our algorithm a good candidate for satellite FDMA/TDMA applications in the 20-30 GHz band, with a large number of users and bursty transmission.

27/7/29 (Item 2 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2003 Inst for Sci Info. All rts. reserv.

04599700 Genuine Article#: TW134 Number of References: 19

Title: A CMOS MULTICHANNEL IC FOR PULSE TIMING MEASUREMENTS WITH 1-MV SENSITIVITY

Author(s): LOINAZ MJ; WOOLEY BA

Corporate Source: AT&T BELL LABS,CRAWFORDS CORNER RD/HOLMDEL//NJ/07733;
STANFORD UNIV,CTR INTEGRATED SYST/STANFORD//CA/94305

Journal: IEEE JOURNAL OF SOLID-STATE CIRCUITS, 1995, V30, N12 (DEC), P 1339-1349

ISSN: 0018-9200

Language: ENGLISH Document Type: ARTICLE

Abstract: A multichannel data acquisition circuit that measures the occurrence times of input pulses relative to a 62.5-MHz clock has been integrated in a 1.2-mu m CMOS technology, The pulse timing measurement channels are sensitive to input pulses with peak amplitudes as small as 1 mV, Each channel consists of a wideband preamplifier, a tail-cancellation filter, a timing discriminator with time-walk compensation, and a **time** digitizer, A **phase** -locked loop (PLL) reference for the time digitizer is included in the circuit, An overall channel timing error of 0.46 ns RR IS has been achieved, with negligible channel-to-channel crosstalk, at a power dissipation of 50 mW/channel.

27/7/30 (Item 3 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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03337914 Genuine Article#: NY095 Number of References: 13

Title: WAFER FAULT MEASUREMENT BY COHERENT OPTICAL PROCESSOR

Author(s): CAI XY; KVASNIK F; BLORE RW

Corporate Source: UNIV MANCHESTER, INST SCI & TECHNOL, DEPT INSTRUMENTAT & ANALYT SCI/MANCHESTER M60 1QD/LANCS/ENGLAND/

Journal: APPLIED OPTICS, 1994, V33, N20 (JUL 10), P4487-4496

ISSN: 0003-6935

Language: ENGLISH Document Type: ARTICLE

Abstract: A microscope coherent optical processor based on the VanderLugt optical correlator is applied to the measurement of registration error in multilayer **integrated - circuit** wafers. A treatment of the effects of wafer faults on the correlation signal is given. Threshold criteria and fault-induced peak splitting of the correlation **signal** from reject production **samples** are exploited to demonstrate the easy and rapid **detection** of **faults** in partially processed **integrated - circuit** wafers.

27/7/31 (Item 1 from file: 35)

DIALOG(R)File 35:Dissertation Abs Online

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01826956 ORDER NO: AADAA-I3010541

High performance, high speed VLSI architectures for wireless communication applications

Author: Chi, Zhipei

Degree: Ph.D.

Year: 2001

Corporate Source/Institution: University of Minnesota (0130)

Adviser: Keshab K. Parhi

Source: VOLUME 62/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 1502. 175 PAGES

ISBN: 0-493-19919-5

This thesis is devoted to high performance and high speed **VLSI** algorithm and architecture design of wireless transceiver building blocks which perform the two major classes of digital signal processing: adaptive least square filtering and turbo decoding.

Hybrid Annihilation Transformation (HAT) for pipelining QR decomposition (QRD) based least square adaptive filters has been developed. HAT provides a unified framework for the derivation of high-speed **VLSI** architectures of QRD-RLS, QRD-LSL, and QRD multi-channel LSL adaptive filters. In addition, *Generalized annihilation reordering transformation* has been proposed to show that *M* filtering errors can be obtained as smoothed filtering results in one **clock cycle** where *M* is pipelining or parallel processing level. The proposed transformations introduce no performance degradation no matter how deep the filter is pipelined. It allows a linear throughput speedup by linear increase in hardware complexity.

Turbo decoding metrics aided short CRC codes **error detection** algorithm has been developed and applied to short frame terminated turbo codes, novel efficient tail-biting turbo codes and CRC embedded turbo codes to realize adaptive decoding and accommodate ARQ protocols. Significant coding gains can be achieved by actually increasing the transmission rate with negligible increase in power consumption.

In addition to strategies on reducing the complexity of general block turbo decoders, a novel robust sub-optimal decoding algorithm for decoding $(32, 21)$ (extended BCH code over *GF*(2^5)) block turbo codes has been proposed. The algorithm achieves 10^{-6} **bit error**

rate at SNR 2.4 *dB* for AWGN channels, which is the best performance among all 2-D turbo product codes. Top level fully parallel decoding architecture and lower level high speed implementation strategies such as critical path reduction using lookahead techniques and fast finite field operations have been developed. An up to 85 *M* bits/s decoding throughput can be achieved by using 0.18 μm , 1.5V CMOS technology.

Iterative decoding of concatenated space-time trellis codes and convolutional codes has been studied as an initial work for further research. Extra coding gains in addition to the diversity advantage is shown to have been achieved for certain space-time trellis codes transmitted over both quasi-static and fast flat fading channels.

27/7/32 (Item 2 from file: 35)

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01536298 ORDER NO: AAD97-10160

PARAMETER ESTIMATION IN SPREAD-SPECTRUM MULTIPLE-ACCESS COMMUNICATION SYSTEMS (CDMA)

Author: FANG, XIAOLING

Degree: PH.D.

Year: 1996

Corporate Source/Institution: THE UNIVERSITY OF UTAH (0240)

Source: VOLUME 57/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 6444. 115 PAGES

This dissertation **examines** the **problems** of acquisition and **tracking** in multiple-access communication systems. At first an acquisition algorithm is presented by modelling the **samples** of the received **signal**. The **samples** in each bit **time interval** are shown to be the outputs of a bank of linear systems whose coefficients are related to the channel parameters. This acquisition algorithm can acquire the initial timing errors to within one **chip** or a fraction of **chip** time. In addition, the acquisition algorithm explicitly takes all the users into account, so it is not near-far limited. Most importantly, the complex amplitudes can be obtained simultaneously. It is also proven possible to apply this acquisition approach to the case of unknown bit sequences at the expense of increased complexity by using tree-search algorithm. A joint estimator of bit sequences and parameters in the tracking stage is developed and discussed to deal with the **tracking problem** after acquisition. The parameter estimator tracks the coefficients of the matched filter outputs using conventional adaptive algorithms and delays using an EKF (extended Kalman filter). One important feature of this joint estimator is that it can use these well-investigated optimal or suboptimal multiuser receivers to detect the bit sequences jointly. Simulation results show that the complex amplitudes and delays can be tracked accurately. Finally, the scheme of a complete multiuser receiver for DS/SSMA systems with unknown parameters is obtained and investigated by combining the proposed acquisition algorithm and joint estimator.

27/7/33 (Item 3 from file: 35)

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01454907 ORDER NO: AADAA-I9544160

SYSTEM ANALYSIS AND DESIGN OF HIGH-SPEED LOCAL AREA NETWORK TRANSCEIVERS (ETHERNET, SIGNAL PROCESSING)

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Chair: HENRY SAMUELI
Source: VOLUME 56/09-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 5051. 139 PAGES

The next generation of Local Area Networks will operate at data rates up to ten times those of current day networks. In order to keep the costs of implementing these networks at a minimum, designers are attempting to use simple unshielded twisted pair wire (similar to telephone wire) to connect network terminals to the central hub. Due to the large amount of noise, attenuation, and distortion present on long stretches of this type of wire, advanced signal processing techniques, such as noise cancellation and channel equalization, are required in order to receive with minimum errors made. This project has investigated several signal processing algorithms that will be useful in the design of transceivers for next generation LANs, such as the proposed 100Base-T4 Ethernet scheme.

Category 3 Unshielded Twisted Pair (UTP) cables are the most prevalent and inexpensive cables capable of sustaining data rates up to 100 Mbit/s. Due to the distortion present on long stretches of Category 3 cables, innovative encoding schemes, **error checking** algorithms, and redundancy had to be incorporated into the specifications for 100Base-T4. In order to meet the stringent **bit - error** -rate specifications tolerated by Ethernet, designers of 100Base-T4 receivers are required to use complex analog equalization methods to reduce the impairments due to the wire channel.

Until this point, the use of digital equalization techniques has not been considered. This project proposes to use the advanced techniques available in the digital domain to both equalize the channel, and acquire the **clock phase** of every incoming packet. This research project investigates the use of digital adaptive equalization to decrease the effects of distortion on long cables. The parameters necessary for implementation of the adaptive equalizer are determined through extensive simulations using Comdisco's Signal Processing Worksystem (SPW) software.

In addition, a fast and reliable phase acquisition scheme is required in the implementation of a 100Base-T4 transceiver. An innovative use of the Transition Tracking algorithm is presented, and the requisite implementation parameters are determined.

In combination, these digital algorithms allow a single **integrated circuit** to be created that performs the full functionality of a 100Base-T4 Ethernet transceiver at a low cost.

27/7/34 (Item 4 from file: 35)
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0979216 ORDER NO: AAD88-00565
A DEVICE FOR ADAPTIVE SAMPLING IN REAL-TIME USING THE FAN ALGORITHM
Author: BOHS, LAURENCE NEAL
Degree: PH.D
Year: 1987
Corporate Source/Institution: DUKE UNIVERSITY (0066)
Source: VOLUME 48/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 3350. 182 PAGES

Adaptive sampling of cardiac waveforms can produce higher quality measurements than uniform sampling at the same average rates. In retrospective studies of previously recorded cardiac signals, the Fan

algorithm was shown to be the best adaptive sampling method. The Fan selects only those samples necessary for reconstruction of an original signal within a specified peak error or tolerance, and requires storage of both samples and **time intervals** between samples since the latter are irregular. The purpose of this work was to design a device for real-time adaptive sampling with the following characteristics: (1) sample selection according to the Fan algorithm; (2) transmission of data at a given fixed rate; (3) selection of samples providing the lowest peak error for the given fixed rate; and (4) transmission of uniform samples instead of Fan samples if the former provide lower peak error.

A prototype has been constructed using two Texas Instruments TMS32010 signal processors and 81 additional TTL **integrated circuits**. The device initially **samples signals** at up to 16000 samples per second (sps), selects **samples** from this **input stream** according to the Fan algorithm, and transmits the samples and **time intervals** at a specified fixed rate. One-second records of original samples are temporarily stored in buffers for Fan pre-processing. Each record is scanned several times with different Fan tolerances in an attempt to find the lowest tolerance that will allow transmission of samples and **time intervals** at a rate not exceeding the fixed rate. The tolerance after each scan varies according to a linear interpolation algorithm. Five scans are completed when the initial sampling rate is 16000 sps.

The performance of the prototype is characterized using a set of specifically developed test signals. Reconstructed waveforms are also shown in response to three human electrocardiograms and an extracellular cardiac signal. The prototype satisfies the goals of this work, with the **exception** that five pre- **scans** are not always sufficient to guarantee selection of the samples that give the lowest error for each **data** record. However, adaptive **sampling** of electrocardiograms with the prototype produced waveforms with 2-20 times lower peak errors than uniform **sampling** of the same **signals** at the same fixed rates.

27/7/35 (Item 5 from file: 35)
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918693 ORDER NO: AAD86-12750
ON THE ANALYSIS OF SYSTOLIC AND SYSTOLIC-TYPE ARRAYS (PARALLEL COMPUTERS, ARCHITECTURES, VLSI)

Author: JOVER, JUAN-MANUEL
Degree: PH.D.
Year: 1986
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Source: VOLUME 47/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 1198. 118 PAGES

In this dissertation we study synchronous, multiprocessor systems interconnected by fixed links. These special-purpose systems, which we call systolic-type arrays, perform specific algorithms at a higher throughput rate than the sequential architecture of von Neumann. The main contributions of this thesis are the analysis of systolic-type arrays, and the design of one such complex system.

In the **analysis problem** we are given the topology of the network, the function performed by each processor (including timing information), and the input data streams. We want to determine the I/O algorithm performed by the array, and the iteration **interval** (i.e., the **time** between two consecutive **input samples**).

Our solution to the **analysis problem** turns out to be based on the simple, at least in retrospect, observation that analysis is the

reverse of synthesis (design). In design we start with a mathematical algorithm and a representation of it as a signal flow graph (SFG) in which the computations (function evaluations) are represented by delay-free (instantaneous) blocks and the index shifts in the sequences processed by the algorithm are all lumped into so-called z^{-1} blocks. In practice all physical computations take time, which is usually recognized in implementations by assigning a 'long enough' **time** (iteration **interval**) to the z^{-1} blocks to allow all the computations to be executed. In this process, the z^{-1} blocks in the signal flow graph disappear to be replaced either by straight-through interconnections or by actual delays, called shimming delays; such delays may also be necessary at other points in the system.

In the **analysis problem**, we start with a physical implementation described by its computational blocks, their associated processing times, and their interconnections. This can be represented by a so-called logical graph, G . The algorithm performed by the physical circuit can be obtained by reversing the design path: we go from a graph G in which the processing blocks take time to a signal flow graph in which the blocks are instantaneous and all the delays are regrouped into z^{-1} blocks. Then the algorithm can readily be written down from the signal flow graph.

We also present a parallel architecture for the measurement update step of the Kalman filter, which estimates a vector parameter. With a single serial processor, the update of a scalar measurement would take time $O(n^2)$, where n is the vector dimension of the parameter; we present an array with $2n + 4$ elementary processors and a bank of delay units that will carry out the measurement update in time $O(n)$. In addition, we use this architecture to illustrate the power of our analysis procedure.

27/7/36 (Item 1 from file: 94)

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01418783 JICST ACCESSION NUMBER: 92A0027043 FILE SEGMENT: JICST-E
Special Issue on the High Performance ASIC and Microprocessor. A 64b CMOS

Mainframe Execution Unit Macrocell with Error Detecting Circuit.

HAYASHI T (1); DOI T (2); YAMAGISHI M (2); KOIDE K (2); ISHIYAMA A (3);
HIRAMATSU M (3); YAMAGIWA A (4)

(1) Hitachi, Ltd., Kokubunji-shi, JPN; (2) Hitachi, Ltd., Ome-shi, JPN
; (3) Hitachi, Ltd., Ebinashi, JPN; (4) Hitachi, Ltd., Hadano-shi, JPN
IEICE Trans(Inst Electron Inf Commun Eng), 1991, VOL.E74,NO.11,

PAGE.3775-3779, FIG.6, TBL.2, REF.6

JOURNAL NUMBER: F0699BCQ ISSN NO: 0917-1673

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LANGUAGE: English COUNTRY OF PUBLICATION: Japan

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MEDIA TYPE: Printed Publication

ABSTRACT: A 64b CMOS mainframe execution unit macrocell with **error detecting** circuits is proposed. The conventional techniques to maintain high reliability have been the parity checking and the duplication of the ALU(Arithmetic Logic Unit). However, the required time for generating the parity from the sum output of the ALU has been undesirable for high-speed operation. In order to achieve a short ALU delay time, a parity predicting logic structure is newly adopted. By utilizing this structure, a one-bit - **error detecting** function is integrated without duplicating the every ALU circuit. A novel CMOS precharged circuit is also developed to shorten the time required to precharge the whole circuit. When the number of circuit stages is

reduced, the precharge time as well as the delay time restricts the ALU cycle time. This new circuitry solves the precharging time accumulation problem in the conventional circuits. A 64b BCD ALU adopting this technology has been designed and fabricated. The parity predict architecture and the high-speed-precharge circuit have been effective in reducing the delay time by 23% and the precharge time by 42%. A 30% faster cycle time has been achieved with a small increase (4%) in ALU area. The execution unit macrocell, which includes the ALU described above, contains 45k transistors and its area is 4.3mm*4.1mm using the 0.8.MU.m CMOS triple metal layer technology. (author abst.)

27/7/37 (Item 1 from file: 95)

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01002818 I96057454320

Use of DS/SS signaling to mitigate Rayleigh fading in a dense scatterer environment

(Anwendung der DS/SS-Link-Architektur in einer dichten Streuumgebung)

Amoroso, F

Omnipoint Corp., Colorado Springs, CO, USA

IEEE Personal Communications, v3, n2, pp52-61, 1996

Document type: journal article Language: English

Record type: Abstract

ISSN: 1070-9916

ABSTRACT:

The issues discussed are summarised by a minimal checklist which should be applied to any DS/SS link architecture for use in a dense scatterer environment. For effective mitigation of fading the chip interval T , should be at most equal to the RMS delay spread Δ , indeed preferably much smaller. For minimal intersymbol interference the symbol duration $T(\text{ind } s)$ should be much longer than Δ . On a fast-moving antenna platform the distance traversed by the antenna during one symbol interval should be much less than 0.38λ . Otherwise, coherent symbol correlation becomes difficult, and a high irreducible error rate may result. The so-called mean bit error rates are just that. They are probabilistic means over the full range of antenna travel. If the antenna tends to remain stationary or travel very slowly, then perhaps it is more meaningful to speak of the maximum (or worst-case) error rate over a specified large fraction of all antenna locations. The chip stream should be as random as possible; that is, the chip values should be statistically uncorrelated. A chip-matched filter, adaptive to the continual metamorphoses of the arriving chip pulse shape and the mean chip arrival time, is essential to symbol detection at those frequently occurring antenna locations where the received power is a minimum, dispersion is a maximum, and the chip pulses arrive with essentially zero mean value. Such situations crop up roughly once per wavelength of antenna travel. In DPSK signaling the matched filter could be as simple as a single time delay of duration $T(\text{ind } s)$.

27/7/38 (Item 2 from file: 95)

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00857493 E95020165320

Corrected multiple upsets and bit reversals for improved 1-s resolution

measurements

(Verbesserung der Aufloesung zur Bestimmung von Fehlern auf der physischen Speicherflaeche)

Brucker, GJ; Stassinopoulos, EG; Stauffer, CA

NASA/Goddard Space Flight Center, Greenbelt, USA; SES Greenbelt, USA

IEEE Transactions on Nuclear Science, v41, n6 Part II, pp2698-2705, 1994

Document type: journal article Language: English

Record type: Abstract

ISSN: 0018-9499

ABSTRACT:

Previous work has studied the generation of single and multiple errors in control and irradiated static RAM samples (Harris 6504RH) which were exposed to heavy ions for relatively long **intervals of time (minute)**, and read out only after the beam was shut off. The present investigation involved storing 4 k x 1 bit maps every second during 1 min ion exposures at low flux rates of 10(exp 3) ions/cm(exp 2)s in order to reduce the chance of two sequential ions upsetting adjacent upset bit locations in the physical memory plane, which were previously defined to constitute multiple upsets. Improvement in the time resolution of these measurements has provided more accurate estimates of multiple upsets. The results indicate that the percentage of multiples decreased from a high of 17 % in the previous experiment to less than 1 % for this new experimental technique. Consecutive double and triple upsets (reversals of bits) were detected. These were caused by sequential ions hitting the same bit, with one or two reversals of state occurring in a 1-min run. In addition to these results, a status review for these same parts covering 3.5 years of imprint damage recovery is also presented.

27/7/39 (Item 3 from file: 95)

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00821407 I94101451310

A discrete Fourier analyzer based on analog VLSI technology

(Ein diskreter Fourier-Analysator auf der Basis der analogen **VLSI** -Technik)

Kawahito, S; Takeda, K; Nishimura, T; Tadokoro, Y

Fac. of Eng., Toyohashi Univ. of Technol., Japan

IEICE Transactions on Electronics, vE77-C, n7, pp1049-1056, 1994

Document type: journal article Language: English

Record type: Abstract

ISSN: 0916-8524

ABSTRACT:

This paper presents a discrete Fourier analyzer using analog **VLSI** technology. An analog current-mode technique is employed for implementing it by a regular array structure based on the straight-forward discrete Fourier transform (DFT) algorithm. The basic components are a 1-dimensional (1-D) analog current-mode multiplier array for fixed coefficient multiplication, a two-dimensional (2-D) analog switch array and wired summations. The proposed scheme can process speedily N-point DFT in a time proportional to N. Possibility of the realization of the analog DFT **VLSI** based on 1 mu m technology is discussed from the viewpoints of precision, speed, area, and power dissipation. In the case of 1024-point DFT, the standard deviation of the total **error** is **estimated** to be about 2%, the latency, or processing time, is about 110 mu s, and the **signal sample** rate based on a pipeline manner is about 4.7 MHz. A prototype MOS **integrated circuit** of the 16-point multiplier array has been implemented

and a typical operation using the multiplier array has been confirmed.

27/7/40 (Item 4 from file: 95)

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00737129 I93103276220

A 156-Mb/s interface CMOS LSI for ATM switching systems

(Ein 156-Mbit/s-CMOS- LSI -Interface fuer Vermittlungssysteme)

Kozaki, T; Aiki, K; Mori, M; Mizukami, M; Asano, K

Central Res. Lab., Hitachi Ltd., Kokubunji, Japan

IEICE Transactions on Communications, vE76-B, n6, pp684-693, 1993

Document type: journal article Language: English

Record type: Abstract

ISSN: 0916-8516

ABSTRACT:

The authors describe a 0.8 μ m CMOS LSI developed for a 156 Mb/s serial interface in ATM switching systems. A low-swing differential signal level is used to achieve 156-Mb/s data transmission. This new circuit technique is named ALTS (advanced low-level transmission circuit system). Using the LSI, transmission can be achieved between boards or racks through a 10 meter twisted pair cable. The LSI has a 156 Mb/s transmitter-receiver, a serial-to-parallel converter and a parallel-to-serial converter. It performs 19.5 Mb/s parallel data/156 Mb/s serial data conversion and 156 Mb/s serial data transmission. In addition, it has a bit phase synchronizer and cell synchronizer, which enables it to transmit and synchronize serial data without a paralleled clock or a paralleled cell top signal, by distributing a common 156 MHz clock and a common cell top signal to the whole system. The authors evaluate the bit error rate and timing margin on data transmission under several conditions.

27/7/41 (Item 1 from file: 99)

DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

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1747915 H.W. WILSON RECORD NUMBER: BAST94025694

Analysis of an all-digital maximum likelihood carrier phase and clock timing synchronizer for eight phase-shift keying modulation

De Gaudenzi, Riccardo; Vanghi, Vieri

IEEE Transactions on Communications v. 42 pt1 (Feb./Mar./Apr. '94) p. 773-82

DOCUMENT TYPE: Feature Article ISSN: 0090-6778

ABSTRACT: An analysis of an all-digital trellis-coded 8 phase shift keying (8PSK) demodulator well suited for VLSI implementation, including maximum likelihood estimation decision-directed carrier phase and clock timing recovery. When combined with trellis coding, 8PSK modulation is an attractive power and bandwidth efficient modulation technique. Using extensive computer simulations, the phase and timing discriminator characteristic in the presence of estimation bias and thermal noise was analytically derived and checked. The simulation results provided confirmation that the expected performance was close to the Cramer-Rao bound for medium signal-to-noise ratios for both synchronizers. Using the Monte Carlo simulation technique, the mean acquisition time for the digital synchronizer was computed and checked. In practical cases, the effects of residual synchronizer errors on 8PSK demodulator bit error rate were found to be negligible. .

27/7/42 (Item 2 from file: 99)

DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs
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1141973 H.W. WILSON RECORD NUMBER: BAST94010521

A 12.5 Gb/s Si bipolar IC for PRBS generation and bit error detection up to 25 Gb/s

Bussmann, Matthias; Langmann, Ulrich; Hillery, William J
IEEE Journal of Solid-State Circuits v. 28 (Dec. '93) p. 1303-9
DOCUMENT TYPE: Feature Article ISSN: 0018-9200

ABSTRACT: Part of a special issue on analog and signal processing. A silicon bipolar **integrated circuit** (IC) that features pseudorandom binary sequence (PRBS) generation, **bit error detection**, scrambling, and trigger derivation up to 12.5 Gb/s is presented. The proposed single-**chip** PRBS tester is suitable for **test problems** typical for ICs for optical fiber communication systems. The circuit, mounted in a hybrid package, lends itself to a handy device for testing with PRBSs. The following test applications have been demonstrated to date: A 2-by-1 multiplexer has been tested at an output data rate of 25 Gb/s; a 1-by-4 demultiplexer has been characterized at 12.5 Gb/s; and the PRBS IC has been used to test an 8-Gb/s **phase**-locked loop for **clock** recovery. The implementation of Gb/s measurement systems on a single **chip** might be a realistic objective in the near future and this IC is a step in this direction.

27/7/43 (Item 1 from file: 144)

DIALOG(R)File 144:Pascal
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15391867 PASCAL No.: 02-0080680

A 0.6-2.5-GBaud CMOS tracked 3x oversampling transceiver with dead-zone phase detection for robust clock /data recovery

MOON Y; JEONG D K; AHN G

Seoul National University ISRC, Seoul 151-742, Korea, Republic of
Journal: IEEE Journal of Solid-State Circuits, 2001, 36 (12) 1974-1983
ISSN: 0018-9200 CODEN: IJSCBC Availability: INIST-222 L
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Document Type: P (Serial) ; A (Analytic)

Country of Publication: United States

Language: English

For generation of the multiphase clocks for a serializer, a wide-range multiphase delay-locked loop (DLL) is used in the transmitter to avoid the detrimental characteristics of a phase-locked loop (PLL), such as jitter peaking and accumulated phase **error**. A **tracked** 3x oversampling technique with dead-zone phase detection is incorporated in the receiver for robust clock/data recovery in the presence of excessive jitter and intersymbol interference (ISI). Due to the dead-zone phase detection, phase adjustment is performed only on the tail portions of the transition histogram in the received data eye, thereby exhibiting wide pumping-current range, large jitter tolerance, and small phase error. A voltage-controlled oscillator (VCO), based on a folded starved inverter, shows about 50% less jitter than one with replica bias. The transceiver, implemented in 0.25- μ m CMOS technology, operates at 2.5 GBaud over a 10-m 150- Ω OMEGA STP cable and at 1.25 GBaud over a 25-m cable with a **bit error** rate (BER) of less than 10⁻¹³.

27/7/44 (Item 2 from file: 144)
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15115655 PASCAL No.: 01-0276449

Reliability data analysis software development

Microelectronic yield, reliability, and advanced packaging : Singapore,
28-30 November 2000

GUAN ZHANG; CHER MING TAN

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International Society for Optical Engineering, Bellingham WA, United
States

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Document Type: P (Serial); C (Conference Proceedings) ; A (Analytic)

Country of Publication: United States

Language: English

Reliability is one of the major keys in product development. While reliability tests are conducted in almost every manufacturing plant, the analysis of reliability test data is hardly rigorous, and engineers mainly rely on the softwares that come with the reliability test equipment to perform the test data analysis. Although this is usually sufficient, the underlying assumptions of the analysis are seldom known, and misleading conclusions might be resulted. Also, the sample size for a reliability test is generally determined from an engineering specification, and variation cannot be made when special circumstances arise. Furthermore, confidence interval estimation of MTTF and T SUB 5 SUB 0 , outlier points identification from test data are usually not given. This could make the test analysis meaningless since point estimate can lead to erroneous decision, and so are the outlier points. In addition, a specified distribution, in particular, the exponential distribution is usually assumed in the data **analysis** . However, in practical **problem** , reliability **test** may be affected by other **failure** mechanisms. Thus, **test** data could be from mixture of distributions, and different models need to be identified and analyzed separately. Therefore, to ensure that the reliability test data can be analyzed accurately, the analysis must include sample size determination, parameter and confidence interval estimations, outlier point **identification** , and **failure** mode **identification** . Sample size determination is required so that desirable confidence level can be obtained from test data with acceptable confidence interval. Outlier point identification is required so that undesirable data points can be eliminated and correct analysis for the remaining desirable test data can be done. **Failure** mode **identification** is required so that each **failure** mode can be **analyzed** separately as they tend to have different life distributions. In this paper, reliability data analysis software developed by us will be presented that take into account of the above-mentioned, and hence an accurate and complete reliability test data analysis can be performed.

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S8	732307	IMBALANC? OR EXCEPTION? ? OR DISTORT? OR DEGRAD? OR DISPAR- AT?
S9	339857	S6:S8(3N) (DETECT? OR DISCERN? OR FIND??? ? OR FOUND OR UNC- OVER? OR UN()COVER? OR CHECK? OR CHEQU? OR DIAGNOS? OR LOOK??? ? OR SEEK??? ?)
S10	295185	S6:S8(3N) (PROBE? ? OR PROBING OR SEARCH? OR ESTIMAT? OR EV- ALUAT? OR SURVEY? OR ANALYS? OR ANALYZ? OR ANALYT? OR ASSESS? OR EXAMIN? OR LOCAT? OR REVIEW? OR IDENTIFIC? OR IDENTIFIE? OR IDENTIFY?)
S11	78253	S6:S8(3N) (DISCRIMINAT? OR SCRUTIN? OR DIFFERENTIAT? OR SCR- EEN? OR PINPOINT? OR PIN()POINT??? ? OR RECOGNIT? OR RECOGNIS? OR RECOGNIZ?)
S12	177964	S6:S8(3N) (ASCERTAIN? OR INSPECT? OR DISTINGUISH? OR MONITO- R? OR TRACK? OR TROUBLESHOOT? OR TROUBLE()SHOOT? OR SCAN OR S- CANS OR SCANN??? ? OR TEST??? ?)
S13	2447	SELFTEST? OR SELFDIAGNOS? OR BIST
S14	1220035	IC OR ICS OR INTEGRAT?? ?(1W) (CIRCUIT? OR OPTOELECTRONIC? - OR OPTO()ELECTRONIC? ?) OR CHIP OR CHIPS OR MICROCIRCUIT? OR - MICROELECTRONIC? ?
S15	173814	MICRO() (CIRCUIT? OR ELECTRONIC? ?) OR PRINTED(1W)CIRCUIT? - OR MICROCHIP?
S16	184922	ASI OR ASIC OR VLSI OR VLSIC OR ULSI OR ULSIC OR VHSI OR V- HSIC OR SOI OR SOIC OR MSI OR MSIC OR LSI OR LSIC
S17	6468	S3(S) (S5 OR S9:S13)
S18	307	S17(S)S14:S16
S19	33618	S4(3N) (DATA OR INPUT? OR SIGNAL? ? OR TRAFFIC? OR DATASTRE- AM? OR STREAM?)
S20	41624	BER OR BERT OR (BIT OR BITS OR MULTIBIT? ?) (2N)ERROR?
S21	3	S18(S)S19

S22 8 S18(S)S20
 S23 11 S21:S22
 S24 0 S23/2002:2003
 S25 6 RD S23 (unique items)
 S26 17 S18(S)S4
 S27 0 S26/2002:2003
 S28 21 S25:S26
 S29 17 RD (unique items)
 ? t29/3,k/3,7-11

29/3,K/3 (Item 3 from file: 16)
 DIALOG(R)File 16:Gale Group PROMT(R)
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04361419 Supplier Number: 46396658 (USE FORMAT 7 FOR FULLTEXT)
IMP INTRODUCES FIRST PROGRAMMABLE IC TO MONITOR ANALOG SIGNALS
 News Release, pN/A
 May 20, 1996
 Language: English Record Type: Fulltext
 Document Type: Magazine/Journal; Trade
 Word Count: 1380

(USE FORMAT 7 FOR FULLTEXT)
 TEXT:

...May 20, 1996 -- IMP, Inc. today announced the first UserProgrammable Monitoring and Diagnostic Data Acquisition **Integrated Circuit (IC)**, which is the second member of its Electrically Programmable Analog Circuit (EPAC) family. The IMP50E30 integrates the functions of over 18 discrete analog and digital CMOS **IC** components to provide the most flexible solution available today for monitoring the status of analog signals, **detecting** system **faults**, supporting preventative maintenance, or advising the level of system perishables and consumables. Programmable analog and...

...inputs. Four inputs feature an extended + 16.5V input range through a user selectable on- **chip** 8-times attenuator and level shifter. This capability allows the MP50E30 to operate from a...

...controlled through an external hardware control pin. The IMP50E30 operates as a switched capacitor-based **sampled data** system. Following the input multiplexer is a low-pass anti-alias filter which also removes glitches and noise from incoming signals. A software command configures the **chip** for either the default on- **chip** 15kHz cut-off limit or for an external capacitor-set cut-off frequency limit. The...

...decide to operate without filtering through software commands issued over the serial interface. An on- **chip** timing unit lets the user compensate for filter settling time by programming hold time for...

...more complex window comparison detectors. The user can program the circuit trip-points through on- **chip** 8-bit DACs. As with all EPAC circuits, the functional set-ups and programmed limits are stored in on- **chip** EEPROM memory but can be changed "on-the-fly", in real time, through the **chip** 's Static RAM (SRAM) resource to meet changing system needs. With the connectivity module, a...

...and service activities by giving equipment and system manufacturers a low cost and easily programmable **chip** specifically designed to monitor, diagnose and flag out-of-bound conditions in equipment. For example...

...or wireless paging service. The MP50E30 also finds applications in industrial environments. Equipment condition, operating **time** or **cycles**, or specific performance variables can be monitored so that maintenance people are notified automatically when...can be reprogrammed in-circuit, specialized service or diagnostic routines could be loaded into the **chip** by a service technician to aid system check-out. With equipment that includes the IM...

...lead PLCC package. Pricing starts at \$9.36 in 1,000-unit quantities. Devices and **samples** are available now. Industrial temperature range devices and 44-pin MQFP packaged devices are in...

...Nasdaq: IMPX) is a leading supplier of high-integration and programmable, analog and mixed-signal **integrated circuits** for computer, communications and control applications. IMP is a technology leader in the field of...

29/3,K/7 (Item 3 from file: 148)

DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2003 The Gale Group. All rts. reserv.

06223053 SUPPLIER NUMBER: 14206501 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Disk-drive controllers automate data flow; embedded controllers remove the hard-drive microcontroller's data-flow burden on AT and SCSI buses.
(Ideas for Design) (Tutorial)

Nass, Richard

Electronic Design, v40, n20, p79(4)

Oct 1, 1992

DOCUMENT TYPE: Tutorial ISSN: 0013-4872 LANGUAGE: ENGLISH

RECORD TYPE: FULLTEXT; ABSTRACT

WORD COUNT: 2124 LINE COUNT: 00172

... from emptying.

The family's error-detection-and-correction block supports standard 32- and 56- **bit** computer-generated **error** -correction codes (ECCs) and an 88-bit non-interleaved Reed-Solomon code (all fixed). In...

...32-bit code requires microcontroller assistance for all correction while the 56- and 88-bit **ECC** implementations offer on-the-fly, as well as microcontroller-assisted (off-line), correction. In the on-the-fly mode, the **chips** can correct a single-burst error of up to 14 bits using the 88-bit Reed-Solomon code or up to 11 bits using the 56-bit **ECC**. Because the **error - detection** -and-correction logic isn't shared, the **chips** can read and correct errors in adjacent sectors without slipping a revolution. All on-the-fly corrections are done within half of a **sector time**.

The chips offer a wide range of control for power modes. The power manager offers...

29/3,K/8 (Item 4 from file: 148)

DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2003 The Gale Group. All rts. reserv.

05583069 SUPPLIER NUMBER: 11679658 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Drive controller simplifies embedded ISA and EISA interfaces. (Extended Industry Standard Architecture) (Adaptec Inc's AIC-8060 intelligent disk controller) (Product Announcement)

Bursky, Dave

Electronic Design, v39, n19, p146(2)

Oct 10, 1991

DOCUMENT TYPE: Product Announcement ISSN: 0013-4872 LANGUAGE:
ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 687 LINE COUNT: 00053

... up to 10 Mbytes/s are supported with 16-bit transfer for data and 8-bit transfers for **error checking** and correction bytes on the host bus. The **chip** can support any AT-bus interface speed thanks to programmable and automatic wait-state insertion. The on-**chip** **ECC** circuits **detect** and correct **errors** in the disk data stream as the data is read from the disk. The **chip** can generate a 32- or 56-bit fixed polynomial **ECC** or an 88-bit Reed-Solomon **ECC** code for the data field and a 16-bit CRC-CCITT for the header field. The on-**chip** hardware performs autocorrection of a sector within a 1/2 **sector time**. The **chip** supports an 8 or 16-bit parallel interface mode and a direct-memory access mode with an on-**chip** slave DMA controller. An on-**chip** 16-byte speed-matching FIFO register between the host port and the data buffer maximizes...

...daisy-chaining two embedded disk controller drives on PC AT is also included on the **chip**. Programmable power-down modes let the **chip** reduce system power while nonactive.

Up to 256 kbytes of external static RAM can be...

29/3,K/9 (Item 5 from file: 148)

DIALOG(R) File 148:Gale Group Trade & Industry DB
(c)2003 The Gale Group. All rts. reserv.

05433425 SUPPLIER NUMBER: 11100994 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Programmable controllers. (Instruments & Controls) (The 1991 Plant Engineering Encyclopedia)
Plant Engineering, v45, n14, p262(6)
July 18, 1991
ISSN: 0032-082X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 4094 LINE COUNT: 00331

... memory locations or data files for use in data manipulation or data handling. Adapter module - **Printed circuit** card that provides communications between an I/O rack and the processor. It transmits I...

...unit, it becomes a rack whenever modules are installed. Checksum - One of several types of **error detection** techniques for ensuring the security of data during storage in memory or during serial transmission...

...without wraparound and carries) and the result is then stored for evaluation later. Circuit card - **Printed circuit** board containing electronic components. Clock - Pulse generator that synchronizes the timing of various logic circuits and memory in the processor. Complementary metal oxide semiconductor (CMOS) - **Integrated circuit** family with high noise immunity and low power consumption. It is especially useful in remote... second occurring in various electronic devices. The standard unit of measure is Hz (hertz), for **cycles per second**. Hexadecimal - Numbering system that represents all possible ON/OFF combinations of four bits with sixteen...signal variation; integral control causes the output signal to change according to the summation of **input signal** values **sampled** up to the present time; and derivative control causes the output signal to change according to the rate at which input signal variations occur during a specific **time interval**. Port - I/O connection on a processor peripheral device. Preset - Upper limit specified for a...

...relative to its channel number and address index position.
Transistor/transistor logic (TTL) Family of **integrated circuit** logic
designed to operate on 5 V power supplies. Voltage levels greater than 2.4
...

29/3,K/10 (Item 6 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2003 The Gale Group. All rts. reserv.

04619981 SUPPLIER NUMBER: 08733386 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**SCSI controller moves synchronous data at 10Mbytes/s: adding intelligence
to peripherals, a highly integrated SCSI controller chip offloads host
computer systems. (Adaptec Inc offers the AIC9110 SCSI controller)**

Bursky, Dave
Electronic Design, v38, n7, p195(3)
April 12, 1990
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1452 LINE COUNT: 00111

... track-write operations are possible because the SCSI circuit's
buffer management block controls off-**chip** buffers of up to 4 Mbytes of
page-mode dynamic RAM (DRAM) and 256 kbytes of static RAM (SRAM). To ensure
the serial data's integrity, the **chip** includes an 88-**bit**, Reed-Solomon
error-correction algorithm implemented in hardware for on-the-fly
correction. The circuit also has 32-or 56-**bit error - checking** and
correction capability as well as a 16-bit cyclic-redundancy-checking
option. With hardware, a sector's error corrections can be done within half
a **sector time**.

The chip has four subsections: disk control, buffer control,
SCSI-bus-interface manager, and microprocessor...

29/3,K/11 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)
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01709622
NEC To Market 6 6 MIPS 32-Bit MPU.
COMLINE ELECTRONICS April 10, 1987 p. 11

In June, NEC Corp. (6701) will begin shipping **samples** of its "V70
(microPD70632)" 32-bit microprocessor. The **chip**, which NEC developed,
has a maximum processing speed of 6.6 MIPS and is software...

... double layer CMOS process, and it consumes 1.5 W of powerP Included on
the **chip** is a virtual memory management unit (MMU), a floating-point
arithmetic processor, a high-speed multitasking function, on-**chip fault
detection**, emulation modes for the company's V20 through V50 series
MPUs, and a 6 step...

...can transfer data at 40 MB/sec using its 32-bit external bus and two
clock bus cycle. The MPU can physically address 4 GB.

For software, NEC will offer UNIX System V...

?

File 696:DIALOG Telecom. Newsletters 1995-2003/Oct 14
(c) 2003 The Dialog Corp.
File 15:ABI/Inform(R) 1971-2003/Oct 13
(c) 2003 ProQuest Info&Learning
File 98:General Sci Abs/Full-Text 1984-2003/Sep
(c) 2003 The HW Wilson Co.
File 484:Periodical Abs Plustext 1986-2003/Oct W1
(c) 2003 ProQuest
File 813:PR Newswire 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2003/Oct 15
(c) 2003 PR Newswire Association Inc
File 635:Business Dateline(R) 1985-2003/Oct 13
(c) 2003 ProQuest Info&Learning
File 810:Business Wire 1986-1999/Feb 28
(c) 1999 Business Wire
File 610:Business Wire 1999-2003/Oct 15
(c) 2003 Business Wire.
File 369:New Scientist 1994-2003/Oct W1
(c) 2003 Reed Business Information Ltd.
File 370:Science 1996-1999/Jul W3
(c) 1999 AAAS
File 20:Dialog Global Reporter 1997-2003/Oct 15
(c) 2003 The Dialog Corp.
File 624:McGraw-Hill Publications 1985-2003/Oct 15
(c) 2003 McGraw-Hill Co. Inc
File 634:San Jose Mercury Jun 1985-2003/Oct 14
(c) 2003 San Jose Mercury News
File 647:CMP Computer Fulltext 1988-2003/Sep W3
(c) 2003 CMP Media, LLC
File 674:Computer News Fulltext 1989-2003/Oct W1
(c) 2003 IDG Communications

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Set	Items	Description
S1	11543600	TIME OR TIMING OR TIMER? ? OR CLOCK??? ? OR TEMPORAL
S2	6631373	MINUTE? ? OR SECOND? ?
S3	645205	S1:S2(3N) (INTERVAL? ? OR PHASE OR PHASES OR ZONE OR ZONES - OR PERIOD? ? OR CYCLE OR CYCLES OR SECTOR? ? OR DURATION? OR - STAGE OR STAGES)
S4	648004	SAMPLE? OR SAMPLING?
S5	13296	ECC OR EDAC
S6	7498073	INVALID? OR MISTAK? OR FAIL? OR PROBLEM? OR FAULT? OR DEFE- CT? OR DEFICIEN? OR ABNORMA? OR FLAW? OR ABERRA? OR MALFUNCTI- ON?
S7	1946704	INOPERA? OR UNUSUAL OR DYSFUNCTION? OR DISFUNCTION? OR BUG? ? OR DETERIORAT? OR ATYPICAL? OR ERROR? ? OR DEVIA? OR IRREG- ULAR? OR CORRUPT?
S8	852687	IMBALANC? OR EXCEPTION? ? OR DISTORT? OR DEGRAD? OR DISPAR- AT?
S9	400146	S6:S8(3N) (DETECT? OR DISCERN? OR FIND??? ? OR FOUND OR UNC- OVER? OR UN()COVER? OR CHECK? OR CHEQU? OR DIAGNOS? OR LOOK??? ? OR SEEK??? ?)
S10	339636	S6:S8(3N) (PROBE? ? OR PROBING OR SEARCH? OR ESTIMAT? OR EV- ALUAT? OR SURVEY? OR ANALYS? OR ANALYZ? OR ANALYT? OR ASSESS? OR EXAMIN? OR LOCAT? OR REVIEW? OR IDENTIFIC? OR IDENTIFIE? OR IDENTIFY?)
S11	94165	S6:S8(3N) (DISCRIMINAT? OR SCRUTIN? OR DIFFERENTIAT? OR SCR- EEN? OR PINPOINT? OR PIN()POINT??? ? OR RECOGNIT? OR RECOGNIS? OR RECOGNIZ?)
S12	167277	S6:S8(3N) (ASCERTAIN? OR INSPECT? OR DISTINGUISH? OR MONITO-

R? OR TRACK? OR TROUBLESHOOT? OR TROUBLE()SHOOT? OR SCAN OR S-
 CANS OR SCANN??? ? OR TEST??? ?)
 S13 1612 SELFTEST? OR SELFDIAGNOS? OR BIST
 S14 891065 IC OR ICS OR INTEGRAT?? ?(1W) (CIRCUIT? OR OPTOELECTRONIC? -
 OR OPTO()ELECTRONIC? ?) OR CHIP OR CHIPS OR MICROCIRCUIT? OR -
 MICROELECTRONIC? ?
 S15 91711 MICRO() (CIRCUIT? OR ELECTRONIC? ?) OR PRINTED(1W)CIRCUIT? -
 OR MICROCHIP?
 S16 118090 ASI OR ASIC OR VLSI OR VLSIC OR ULSI OR ULSIC OR VHSI OR V-
 HSIC OR SOI OR SOIC OR MSI OR MSIC OR LSI OR LSIC
 S17 7195 S3(S) (S5 OR S9:S13)
 S18 185 S17(S)S14:S16
 S19 12 S18(S)S4
 S20 44989 BER OR BERT OR (BIT OR BITS OR MULTIBIT? ?) (2N)ERROR?
 S21 4 S18(S)S20
 S22 14 S19 OR S21
 S23 3 S22/2002:2003
 S24 11 S22 NOT S23
 S25 10 RD (unique items)

25/3,K/10 (Item 2 from file: 674)
DIALOG(R)File 674:Computer News Fulltext
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042166

**Server searching: a game of break the bottleneck
Buyers Guide**

Byline: Tony Croes and Josh Penrod
Journal: Network World Page Number: 33
Publication Date: January 30, 1995
Word Count: 4491 Line Count: 423

Text:

... PC-based servers use Complex Instruction Set Computing (CISC) or Reduced Instruction Set Computing (RISC) **chips** and support industry-standard PC I/O buses, such as Extended Industry Standard Architecture (EISA...

... the PC-based server market with products that use RISC or scalable processor architecture (SPARC) **chips**. With so many advances being foisted upon you, the initial temptation is to plow through...

... numerous fault-tolerant features designed to provide maximum server availability. Prevalent high-end features include **error checking** and correcting (**ECC**) memory, which maintains the integrity of data in random-access memory and stored on disk...

... have large storage and memory capacities, as well as segmented bus architectures. Support for multiprocessing, **ECC** memory and other fault-tolerant features often cost more. At the low end, a new...

... servers to work in ASMP mode. There are also arguments about whether CISC or RISC **chips** perform better, but that debate is abating (see story, this page). Both types of **chips** see performance gains as the number of transistors that can be placed on them. As CPU **chips** become more dense with transistors, the performance gains typically outpace the ability of main memory... data is being fetched from memory. The process of fetching data from memory requires a **cycle** of **time** on the CPU-to-memory bus. In a nonpipelined architecture, a **second cycle** is not started until the first one completes, and there is a time delay before the **second cycle** starts. In a pipelined bus architecture, the **second cycle** begins before the first cycle completes. This way, the data from the **second cycle** is available immediately after the completion of the first cycle. Pipelining is found on Digital...Multichannel, intelligent, Fast SCSI-2 array controllers will become the norm for all servers. However, **look** for **fault** -tolerant features such as battery backups and posted write-back cache to remain differentiating features... take fault-tolerant and management features for granted, because they are not all alike. Take **ECC** memory, for example. Most vendors support **ECC** for single **bit** memory **errors** - the most common type. When there are memory errors that exceed a single bit, these servers generate a nonmaskable interrupt and halt processing. Vendors such as Compaq use advanced **ECC** memory to **detect** and correct **errors** to as many as four adjacent bits. This means that an entire **chip** could fail and the Compaq server would continue to run. In addition to **ECC**, there are a number of **fault** -tolerant features to **look** for, including automatic server restart after a system **failure**, automatic drive **monitoring** and drive repair, parity checks across internal data paths, hot spares and redundancy, as well...

... than they do because of component or subsystem failure. A comprehensive management strategy that encompasses **problem** prevention, **detection** and recovery is as important as any feature implemented in hardware. This is why many... Intel, AMD Co., Cyrix Corp. and NextGen in the Pentium-class processor market will drive **chip** prices through the floor. At the same time, server vendors will try to achieve better cost and performance with multiple Pentium-class microprocessors than what the next-generation **chips** will deliver. The long and the short is that the market may not be so...

File 256:SoftBase:Reviews,Companies&Prods. 82-2003/Sep
(c)2003 Info.Sources Inc

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Set	Items	Description
S1	21812	TIME OR TIMING OR TIMER? ? OR CLOCK??? ? OR TEMPORAL
S2	4643	MINUTE? ? OR SECOND? ?
S3	787	S1:S2(3N) (INTERVAL? ? OR PHASE OR PHASES OR ZONE OR ZONES - OR PERIOD? ? OR CYCLE OR CYCLES OR SECTOR? ? OR DURATION? OR - STAGE OR STAGES)
S4	1607	SAMPLE? OR SAMPLING?
S5	20	ECC OR EDAC
S6	13773	INVALID? OR MISTAK? OR FAIL? OR PROBLEM? OR FAULT? OR DEFE- CT? OR DEFICIEN? OR ABNORMA? OR FLAW? OR ABERRA? OR MALFUNCTI- ON?
S7	4522	INOPERA? OR UNUSUAL OR DYSFUNCTION? OR DISFUNCTION? OR BUG? ? OR DETERIORAT? OR ATYPICAL? OR ERROR? ? OR DEVIA? OR IRREG- ULAR? OR CORRUPT?
S8	1892	IMBALANC? OR EXCEPTION? ? OR DISTORT? OR DEGRAD? OR DISPAR- AT?
S9	1552	S6:S8(3N) (DETECT? OR DISCERN? OR FIND??? ? OR FOUND OR UNC- OVER? OR UN()COVER? OR CHECK? OR CHEQU? OR DIAGNOS? OR LOOK??? ? OR SEEK??? ?)
S10	1155	S6:S8(3N) (PROBE? ? OR PROBING OR SEARCH? OR ESTIMAT? OR EV- ALUAT? OR SURVEY? OR ANALYS? OR ANALYZ? OR ANALYT? OR ASSESS? OR EXAMIN? OR LOCAT? OR REVIEW? OR IDENTIFIC? OR IDENTIFIE? OR IDENTIFY?)
S11	221	S6:S8(3N) (DISCRIMINAT? OR SCRUTIN? OR DIFFERENTIAT? OR SCR- EEN? OR PINPOINT? OR PIN()POINT??? ? OR RECOGNIT? OR RECOGNIS? OR RECOGNIZ?)
S12	1269	S6:S8(3N) (ASCERTAIN? OR INSPECT? OR DISTINGUISH? OR MONITO- R? OR TRACK? OR TROUBLESHOOT? OR TROUBLE()SHOOT? OR SCAN OR S- CANS OR SCANN??? ? OR TEST??? ?)
S13	9	SELFTEST? OR SELFDIAGNOS? OR BIST
S14	1567	IC OR ICS OR INTEGRAT?? ?(1W) (CIRCUIT? OR OPTOELECTRONIC? - OR OPTO()ELECTRONIC? ?) OR CHIP OR CHIPS OR MICROCIRCUIT? OR - MICROELECTRONIC? ?
S15	545	MICRO() (CIRCUIT? OR ELECTRONIC? ?) OR PRINTED(1W)CIRCUIT? - OR MICROCHIP? OR SEMICOND?
S16	3	SEMI() (COND OR CONDUCT?R? ?) OR FET OR FIELD()EFFECT? ?()D- EVICE? ?
S17	45	S3 AND (S5 OR S9:S13)
S18	2	S17 AND S14:S16
S19	278	ASIC? ? OR VLSI OR ULSI OR VHSI
S20	60	SOIC OR MSI OR LSI
S21	35	VLSIC OR ULSIC OR VHSIC OR MSIC OR LSIC
S22	1	S17 AND S19:S21
S23	2	S18 OR S22

? t23/7/1

23/7/1

DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.
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00107569 DOCUMENT TYPE: Review

PRODUCT NAMES: StyleCheck Windows & UNIX (699004)

TITLE: Quickturn's StyleCheck enforces design discipline
AUTHOR: Santarini, Michael

SOURCE: Electronic Engineering Times, v980 p73(1) Nov 10, 1997
ISSN: 0192-1541
HOMEPAGE: <http://www.eet.com>

RECORD TYPE: Review
REVIEW TYPE: Product Analysis
GRADE: Product Analysis, No Rating

Quickturn Design Systems' StyleCheck, a scan-and-filter IC design tool, ensures that a design team's Verilog code adheres through the entire design flow to a known, verifiable subset of the Verilog language. StyleCheck aims to ensure that standards for good logic design are followed, so that first-pass silicon and faster time-to-market result. Design sizes are now approaching multiple millions of gates, which means that making logic function correctly is more complicated. When **errors** are not **found** in a design, several silicon 'respins' can be the result, a very expensive process when these very large application-specific **integrated circuits** (**ASICs**) are being built. StyleCheck monitors register-transfer level (RTL) Verilog before event-driven simulation, **cycle** -based simulation, static **timing** analysis, synthesis, and emulation to ensure that the code is stable. StyleCheck does this by scanning and filtering code, and by checking to determine that code conforms to Quickturn's 'verifiable subset,' or a refined subset taken by Quickturn from the synthesizable subset of the 1364 IEEE standard Verilog. Using the verification subset, the tool **finds** syntax **errors** in RTL code and reveals design-style **problems** . It can **find** such effects as asynchronous loops, glitch generation logic from flip-flops, and inconsistent clocking.

REVISION DATE: 20001230
?

File 347:JAPIO Oct 1976-2003/Jun(Updated 031006)
 (c) 2003 JPO & JAPIO
 File 350:Derwent WPIX 1963-2003/UD,UM &UP=200365
 (c) 2003 Thomson Derwent
 File 348:EUROPEAN PATENTS 1978-2003/Oct W01
 (c) 2003 European Patent Office
 File 349:PCT FULLTEXT 1979-2002/UB=20031009,UT=20031002
 (c) 2003 WIPO/Univentio

? ds

Set	Items	Description
S1	9	AU='PERROTT M H':AU='PERROTT MICHAEL H'
S2	22048	(BIT OR BITS) (2N)ERROR?
S3	565240	IC OR ICS OR INTEGRAT?? ?(1W)CIRCUIT?
S4	182	S2(20N)S3
S5	0	S1 AND S4
S6	5	S1 AND S2:S3

? t6/9/1-2

6/9/1 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX
 (c) 2003 Thomson Derwent. All rts. reserv.

014561559 **Image available**
 WPI Acc No: 2002-382262/200241
 Related WPI Acc No: 2002-382261
 XRPX Acc No: N02-299225

Digital phase detector circuit for a phase locked loop includes linear phase detector and digital encoder system

Patent Assignee: SILICON LAB INC (SILI-N); PERROTT M H (PERR-I)

Inventor: **PERROTT M H**

Number of Countries: 096 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200205429	A2	20020117	WO 2001US21645	A	20010710	200241 B
AU 200218798	A	20020121	AU 200218798	A	20010710	200241
US 20020033714	A1	20020321	US 2000217207	P	20000710	200241
			US 2000217208	P	20000710	
			US 2001902542	A	20010710	
US 20030020640	A1	20030130	US 2000217207	P	20000710	200311
			US 2000217208	P	20000710	
			US 2001902548	A	20010710	
US 6590426	B2	20030708	US 2000217207	P	20000710	200353
			US 2000217208	P	20000710	
			US 2001902542	A	20010710	

Priority Applications (No Type Date): US 2000217208 P 20000710; US 2000217207 P 20000710; US 2001902542 A 20010710; US 2001902548 A 20010710

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 200205429 A2 E 52 H03L-000/00

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200218798 A H03L-000/00 Based on patent WO 200205429

US 20020033714 A1 H03D-003/00 Provisional application US 2000217207

Provisional application US 2000217208

US 20030020640 A1 H03M-007/00 Provisional application US 2000217207

US 6590426 B2 G01R-029/00 Provisional application US 2000217208
Provisional application US 2000217207
Provisional application US 2000217208

Abstract (Basic): WO 200205429 A2

NOVELTY - A linear phase detector circuit (240) is responsive to a first and second signal and generates an output signal that varies linearly with phase difference between the two signals over a certain range of phase differences. A digital encoder circuit is responsive to the output signal from the linear phase detector and generates a digital phase error signal.

DETAILED DESCRIPTION - The digital encoder circuit generates a digital phase error signal that has quantized timing and magnitude that encodes the phase difference between the two signals.

An INDEPENDENT CLAIM is included for:

(1) a method of generating a digital phase error signal representing the phase error between a first and second signal

USE - For use in phase locked loops and for clock and data recovery circuits.

ADVANTAGE - The system eliminates the need for an external loop filter capacitor and a large loop filter capacitor integrated on the same **integrated circuit** die as the phase locked loop. Therefore, printed wiring board layout issues are simplified.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a digital phase detector.

Linear phase detector circuit (240)

pp; 52 DwgNo 6/14

Title Terms: DIGITAL; PHASE; DETECT; CIRCUIT; PHASE; LOCK; LOOP; LINEAR; PHASE; DETECT; DIGITAL; ENCODE; SYSTEM

Derwent Class: U23

International Patent Class (Main): G01R-029/00; H03D-003/00; H03L-000/00; H03M-007/00

International Patent Class (Additional): H03L-007/06

File Segment: EPI

Manual Codes (EPI/S-X): U23-D01A3A; U23-D01A8B

6/9/2 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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014561558 **Image available**

WPI Acc No: 2002-382261/200241

Related WPI Acc No: 2002-382262

XRPX Acc No: N02-299224

Digitally-synthesized loop filter circuit for a phase locked loop includes digital phase detector, digital accumulator and digital to analog converter system

Patent Assignee: SILICON LAB INC (SILI-N)

Inventor: BAIRD R T; HUANG Y; **PERROTT M H**

Number of Countries: 096 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200205428	A2	20020117	WO 2001US21644	A	20010710	200241 B
AU 200175880	A	20020121	AU 200175880	A	20010710	200241
US 20020089356	A1	20020711	US 2000217207	P	20000710	200248
			US 2000217208	P	20000710	
			US 2001902541	A	20010710	
US 6580376	B2	20030617	US 2000217207	P	20000710	200341

US 2000217208 P 20000710
US 2001902548 A 20010710
Priority Applications (No Type Date): US 2000217208 P 20000710; US
2000217207 P 20000710; US 2001902541 A 20010710; US 2001902548 A 20010710
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 200205428 A2 E 56 H03L-000/00
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA
CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN
IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ
PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR
IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
AU 200175880 A H03L-000/00 Based on patent WO 200205428
US 20020089356 A1 H03B-021/00 Provisional application US 2000217207
Provisional application US 2000217208
US 6580376 B2 H03M-007/00 Provisional application US 2000217207
Provisional application US 2000217208

Abstract (Basic): WO 200205428 A2

NOVELTY - A digital phase detector (202) provides a digital phase error signal. A digital accumulator (212) is responsive to the phase error signal and generates a multi-bit accumulated error signal. A digital to analog converter (214) generates an output signal corresponding to the accumulated error signal for controlling an oscillator within a phase locked loop.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for:

(1) a method of controlling the controlled oscillator
(2) a method of generating an analog output signal delayed by an arbitrarily long time constant from an analog input

USE - For phase locked loops and for clock and data recovery circuits.

ADVANTAGE - The system eliminates the need for an external loop filter capacitor and a loop filter capacitor integrated on the same integrated circuit die. Therefore, the printed wiring board layout issues are simplified.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a phase locked loop circuit incorporating a digitally-synthesized loop filter.

Digital phase detector (202)

Digital accumulator (212)

Digital to analog converter (214)

pp; 56 DwgNo 5/14

Title Terms: DIGITAL; SYNTHESIS; LOOP; FILTER; CIRCUIT; PHASE; LOCK; LOOP;
DIGITAL; PHASE; DETECT; DIGITAL; ACCUMULATOR; DIGITAL; ANALOGUE;
CONVERTER; SYSTEM

Derwent Class: U23

International Patent Class (Main): H03B-021/00; H03L-000/00; H03M-007/00

File Segment: EPI

Manual Codes (EPI/S-X): U23-D01A3A; U23-D01A7; U23-D01A8C

? t6/5/3-5

6/5/3 (Item 1 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00871273 **Image available**

DIGITAL PHASE DETECTOR CIRCUIT AND METHOD THEREFOR

CIRCUIT DE DETECTEUR DE PHASE NUMERIQUE ET PROCEDE CORRESPONDANT

Patent Applicant/Assignee:

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(Residence), US (Nationality)

Inventor(s):

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Legal Representative:

GRAHAM Andrew C (agent), Zagorin, O'brien & Graham, LLP, Suite 870, 401
West 15th Street, Austin, TX 78701, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200205429 A2-A3 20020117 (WO 0205429)

Application: WO 2001US21645 20010710 (PCT/WO US0121645)

Priority Application: US 2000217207 20000710; US 2000217208 20000710

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU

CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP

KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD

SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: H03L-007/085

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 15879

English Abstract

In a feedback system such as a PLL, the integrating function associated with a loop filter capacitor is instead implemented digitally and is easily implemented on the same **integrated circuit** die as the PLL. In a preferred embodiment, an analog phase detector is utilized whose phase error output signal is delta-sigma modulated to encode the magnitude of the phase error using a digital (i.e., discrete-time and discrete-value) signal. This digital phase error signal is "integrated" by a digital integration block including, for example, a digital accumulator, whose output is then converted to an analog signal, optionally combined with a loop feed-forward signal, and then conveyed as a control voltage to the voltage-controlled oscillator. The equivalent "size" of the integrating capacitor function provided by the digital integration block may be varied by increasing or decreasing the bit resolution of circuits within the digital block.

French Abstract

Dans un systeme de retroaction tel qu'une boucle a phase asservie, la fonction d'integration associee a un condensateur de filtre a boucle est mise en oeuvre numeriquement et installee facilement sur la meme puce de circuit integre que la boucle a phase asservie. Selon une realisation preferee, un detecteur de phase analogique, dont le signal de sortie d'erreur de phase est soumis a une modulation delta-sigma, est utilise pour coder la grandeur d'erreur de phase a l'aide d'un signal numerique (c.-a-d. signal a temps discret et a valeur discrete). Ce signal numerique d'erreur de phase est \leq integre \geq par un bloc d'integration numerique comprenant, par exemple, un accumulateur numerique dont la sortie est ensuite convertie en un signal analogique, eventuellement combine a un signal emis en aval, et ensuite envoye sous forme d'une tension de commande a l'oscillateur commande en tension. La \leq dimension \geq equivalente de la fonction d'integration du condensateur obtenue par le bloc d'integration numerique peut varier selon l'augmentation ou la diminution de la resolution binaire des circuits dans le bloc numerique.

Legal Status (Type, Date, Text)

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Examination 20020328 Request for preliminary examination prior to end of
19th month from priority date
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event of the receipt of amendments.

6/5/4 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00871272 **Image available**

**DIGITALLY-SYNTHESIZED LOOP FILTER CIRCUIT PARTICULARLY USEFUL FOR A PHASE
LOCKED LOOP**

**CIRCUIT DE FILTRE A BOUCLE A SYNTHETISATION NUMERIQUE UTILE NOTAMMENT POUR
UNE BOUCLE A PHASE ASSERVIE**

Patent Applicant/Assignee:

SILICON LABORATORIES INC, 4635 Boston Lane, Austin, TX 78735, US, US
(Residence), US (Nationality)

Inventor(s):

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Legal Representative:

GRAHAM Andrew C (et al) (agent), Zagorin, O'Brien & Graham, LLP, Suite
870, 401 West 15th Street, Austin, TX 78701, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200205428 A2-A3 20020117 (WO 0205428)

Application: WO 2001US21644 20010710 (PCT/WO US0121644)

Priority Application: US 2000217207 20000710; US 2000217208 20000710

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CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP

KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD

SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Main International Patent Class: H03L-007/093

Publication Language: English

Filing Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 16897

English Abstract

In a feedback system such as a PLL, the integrating function associated with a loop filter capacitor is instead implemented digitally and is easily implemented on the same **integrated circuit** die as the PLL. In a preferred embodiment, an analog phase detector is utilized whose phase error output signal is delta-sigma modulated to encode the magnitude of the phase error using a digital (i.e., discrete-time and discrete-value) signal. This digital phase error signal is "integrated" by a digital integration block including, for example, a digital accumulator, whose output is then converted to an analog signal, optionally combined with a loop feed-forward signal, and then conveyed as a control voltage to the voltage-controlled oscillator. The equivalent "size" of the integrating

capacitor function provided by the digital integration block may be varied by increasing or decreasing the bit resolution of circuits within the digital block.

French Abstract

Dans un systeme de retroaction tel qu'une boucle a phase asservie, la fonction d'integration associee a un condensateur de filtre a boucle est mise en oeuvre numeriquement et installee facilement sur la meme puce de circuit integre que la boucle a phase asservie. Selon une realisation preferee, un detecteur de phase analogique, dont le signal de sortie d'erreur de phase est soumis a une modulation delta-sigma, est utilise pour coder la grandeur d'erreur de phase a l'aide d'un signal numerique (c.-a-d. signal a temps discret et a valeur discrete). Ce signal numerique d'erreur de phase est \leq integre \geq par un bloc d'integration numerique comprenant, par exemple, un accumulateur numerique dont la sortie est ensuite convertie en un signal analogique, eventuellement combine a un signal emis en aval, et ensuite envoye sous forme d'une tension de commande a l'oscillateur commande en tension. La \leq dimension \geq equivalente de la fonction d'integration du condensateur obtenue par le bloc d'integration numerique peut varier selon l'augmentation ou la diminution de la resolution binaire des circuits dans le bloc numerique.

Legal Status (Type, Date, Text)

Publication 20020117 A2 Without international search report and to be republished upon receipt of that report.
Publication 20020117 A2 Published entirely in electronic form (except the front page) and available upon request from the International Bureau.
Examination 20020328 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20021010 Late publication of international search report
Republication 20021010 A3 With international search report.
Republication 20021010 A3 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
Republication 20021010 A3 Published entirely in electronic form (except the front page) and available upon request from the International Bureau.

6/5/5 (Item 3 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00443875 **Image available**

**DIGITAL COMPENSATION FOR WIDEBAND MODULATION OF A PHASE LOCKED LOOP
FREQUENCY SYNTHESIZER
COMPENSATION NUMERIQUE POUR MODULATION A BANDE LARGE D'UN SYNTHETISEUR DE
FREQUENCE A BOUCLE A PHASE ASSERVIE**

Patent Applicant/Assignee:

MASSACHUSETTS INSTITUTE OF TECHNOLOGY,

Inventor(s):

PERROTT Michael H ,

SODINI Charles G,

CHANDRAKASAN Anantha P

Patent and Priority Information (Country, Number, Date):

Patent: WO 9834339 A1 19980806

Application: WO 98US1612 19980129 (PCT/WO US9801612)

Priority Application: US 97791215 19970131

Designated States: CA JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Main International Patent Class: H03C-003/09

International Patent Class: H04L-27:12; H04L-27:20; H04L-25:03

Publication Language: English

Fulltext Availability:

Detailed Description

Claims

Fulltext Word Count: 15590

English Abstract

A digital compensation filtering technique is provided that enables indirect phase locked loop modulation with a digital modulation data stream having a bandwidth that exceeds, perhaps by an order of magnitude, the bandwidth characteristic of the phase locked loop. A modulation data receiver is provided for receiving from a modulation source digital input modulation data having a bandwidth that exceeds the cutoff frequency characteristic of the phase locked loop frequency response. A digital processor is coupled to the modulation data receiver for digitally processing the input modulation data to amplify modulation data at frequencies higher than the phase locked loop cutoff frequency. This digital processor is connected to the phase locked loop frequency divider to modulate the divider based on the digitally-processed input modulation data, whereby a voltage controlled oscillator of the phase locked loop is controlled to produce a modulated output carrier signal having a modulation bandwidth that exceeds the phase locked loop cutoff frequency. The digital processing of the modulation data can be implemented by adapting a digital FIR Gaussian transmit filter such that its filter characteristic reflects the intended modulation data amplification as well as enables Gaussian Frequency Shift Keyed modulation. With this implementation, no additional componentry beyond the PLL system is needed to implement the digital modulation data processing provided by the invention.

French Abstract

Technique de filtrage a compensation numerique permettant une modulation indirecte de boucle a phase asservie avec un flux de donnees numeriques de modulation dont la largeur de bande depasse, peut-etre par un ordre de grandeur, les caracteristiques de largeur de bande de la boucle a phase asservie. Un recepteur de donnees de modulation sert a recevoir depuis une source de modulation des donnees numeriques de modulation d'entree dont la largeur de bande depasse les caracteristiques de frequence de coupure de la reponse de frequence de boucle a phase asservie. Un processeur numerique est couple au recepteur de donnees de modulation et sert a effectuer le traitement numerique des donnees de modulation d'entree afin d'amplifier les donnees de modulation a des frequences superieures a la frequence de coupure de la boucle a phase asservie. Ce processeur numerique est relie au diviseur de frequence de boucle a phase asservie afin de moduler ce dernier en fonction des donnees de modulation d'entree traitees numeriquement, ce qui permet de commander un oscillateur commande en tension de la boucle a phase asservie afin de produire un signal de porteuse a sortie modulee dont la largeur de bande de modulation depasse la frequence de coupure de la boucle a phase asservie. On peut mettre en oeuvre le traitement numerique des donnees de modulation par adaptation d'un filtre numerique non recursif de transmission gaussienne, de sorte que les caracteristiques de ce dernier reflechissent l'amplification voulue des donnees de modulation et permettent egalement d'effectuer une modulation deplacee en frequence gaussienne. Il n'est, de ce fait, pas necessaire d'ajouter des composants autres que la boucle a phase asservie, afin de mettre en oeuvre ce traitement numerique de donnees de modulation.

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